

CMC26686CX cpuModules™

RTD Enhanced Award BIOS Versions 4.51.xx



User's Manual

BDM-61000062 Revision A

www.rtd.com



An ISO9001:2000 Company

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CMC26686CX *cpuModules*™ User's Manual

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Revision History

Revision	Date	Reason for Change
A	08/20/07	Initial release

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Chapter 1 Introduction

This manual provides comprehensive hardware and software information for users developing with the CMC26686CX PC/104-Plus cpuModule.



Note Read the specifications beginning on page 6 prior to designing with the cpuModule.

This manual is organized as follows:

- Chapter 1** **Introduction**
introduces main features and specifications
- Chapter 2** **Getting Started**
provides abbreviated instructions to get started quickly
- Chapter 3** **Connecting the cpuModule**
provides information on connecting the cpuModule to peripherals
- Chapter 4** **Configuring the cpuModule (BIOS Setup)**
provides information on configuring hardware and software
- Chapter 5** **Using the cpuModule**
provides information to develop applications for the cpuModule, including general cpuModule information, detailed information on storing both applications and system functions, and using utility programs
- Appendix A** **Hardware Reference**
lists jumper locations and settings, physical dimensions, and processor thermal management
- Appendix B** **Troubleshooting**
offers advice on debugging problems with your system
- Appendix C** **IDAN™ Dimensions and Pinout**
provides connector pinouts for the cpuModule installed in an RTD Intelligent Data Acquisition Node (IDAN) frame
- Appendix D** **Additional Information**
lists sources and websites to support the cpuModule installation and configuration
- Appendix E** **Limited Warranty**

CMC26686CX cpuModules

The PC/104-Plus cpuModules described in this manual are designed for industrial applications requiring:

- Software and hardware compatibility with the PC/AT world
- High-speed number-crunching operation
- Low power consumption
- Small physical dimensions
- High reliability
- Good noise immunity

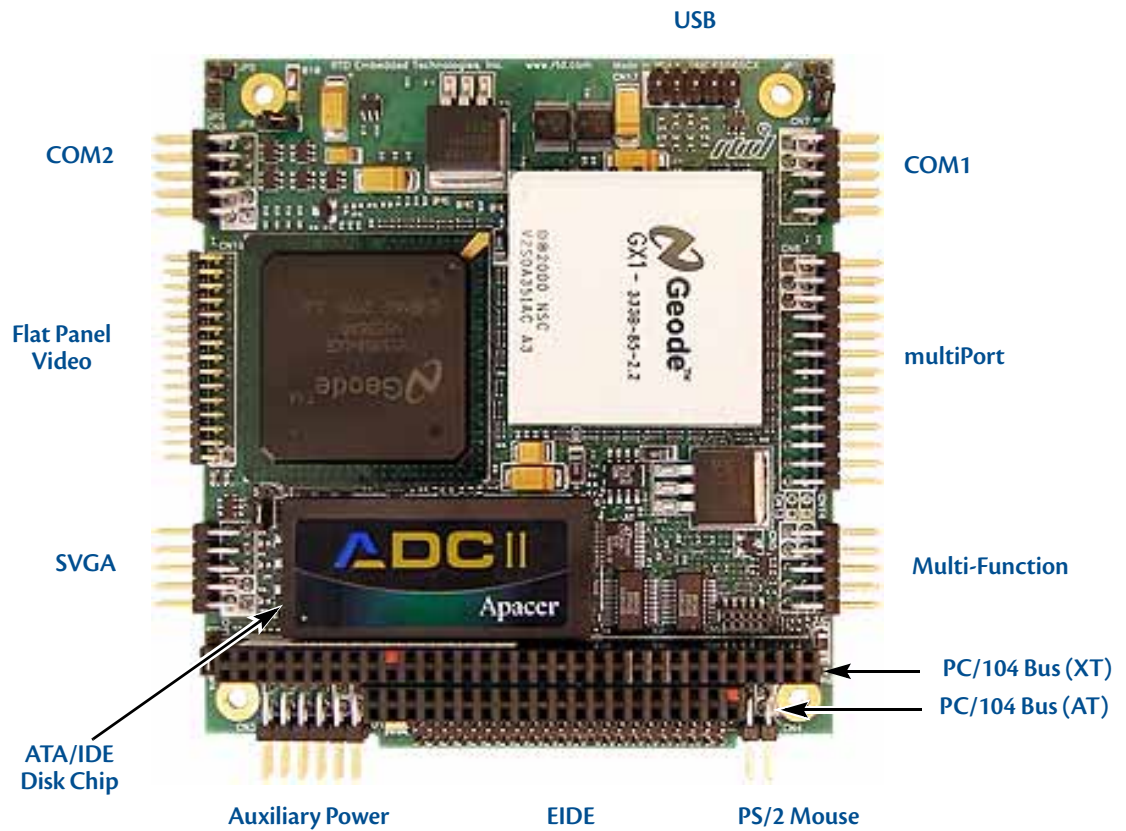


Figure 1 CMC26686CX cpuModule (top view)

Ordering Information

The CMC26686CX cpuModule is available with both 300 and 333 MHz processors and 32, 128, or 256 MB of SDRAM. The cpuModule can also be purchased as part of an Intelligent Data Acquisition Node (IDAN™) building block, which consists of the cpuModule and a milled aluminum IDAN frame. The IDAN building block can be used in just about any combination with other IDAN building blocks to create a simple but rugged PC/104 stack. Refer to Appendix C, *IDAN™ Dimensions and Pinout*, for more information. The CMC26686CX cpuModule can also be purchased as part of a custom-built RTD HiDAN™ or HiDAN*plus* High Reliability Intelligent Data Acquisition Node. Contact RTD for more information on its high reliability PC/PCI-104 systems.

CMC26686CX Model Options

The basic cpuModule model options are shown below. Refer to the RTD website (www.rtd.com) for more detailed ordering information.

Table 1 CMC26686CX cpuModule Model Options

Part Number	Description
CMC26686CX300HR-32	300 MHz, 32 MB SDRAM cpuModule
CMC26686CX300HR-128	300 MHz, 128 MB SDRAM cpuModule
CMC26686CX300HR-256	300 MHz, 256 MB SDRAM cpuModule
CMC26686CX333HR-32	333 MHz, 32 MB SDRAM cpuModule
CMC26686CX333HR-128	333 MHz, 128 MB SDRAM cpuModule
CMC26686CX333HR-256	333 MHz, 256 MB SDRAM cpuModule

Cable Kits and Accessories

For maximum flexibility, RTD does not provide cables with the cpuModule. You may wish to purchase the CMC26686CX cpuModule cable kit (P/N XK-CM70), which contains:

- Multi-function utility cable (keyboard socket, battery, reset, speaker)
- VGA monitor cable (DIL-10 to high density 15-pin DSUB)
- Two serial port cables (DIL-10 to DSUB-9)
- Parallel port cable (DIL-26 to DSUB-25)
- Two USB cables (5-pin SIL to USB A)
- Power cable (DIL-12 to wire leads)
- PS/2 mouse adapter (4-pin DIL to PS/2 female)
- Two IDE cables

A floppy drive cable kit (P/N XK-CM49) is also available for connecting to the multiPort. This cable kit comes with:

- 3.5" HDD Floppy Drive with a multiPort interface board
- Two floppy cables

Board Features

The CMC26686CX cpuModule is highly integrated, combining all major functions of a PC/AT computer on one compact board. It integrates all primary I/O functions of an AT compatible computer, including:

- SVGA controller
- Keyboard interface
- Two RS-232/422/485 serial ports
- One RS-232/422/485 serial port
- Two USB 1.0 ports
- UltraDMA EIDE controller
- Real time clock
- Speaker port
- PS/2 mouse port

It also enhances standard AT-compatible computer systems with the addition of:

- Flat panel video
- 32 pin ATA/IDE Disk Chip Socket
 - Miniature ATA/IDE Flash Disk Chip
 - Capacities up to 4GB¹
 - Natively supported by all major operating systems
- Nonvolatile storage of CMOS settings
- Watchdog timer
- Fail Safe Boot ROM
- multPort™ connector, BIOS selectable as one of the following:
 - Advanced Digital I/O (aDIO™), 16 digital bits configured as 8-bit programmable and 8-bit port programmable I/O, providing any combination of inputs and outputs
 - Parallel port configurable in SPP, ECP, EPP 1.7, and EPP 1.9 operational modes
 - Floppy drive controller

1. During the time of this manual's publication, 4GB was the largest available ATA/IDE Disk Chip capacity

Block Diagram

The next figure shows a simplified block diagram of the CMC26686CX cpuModule.

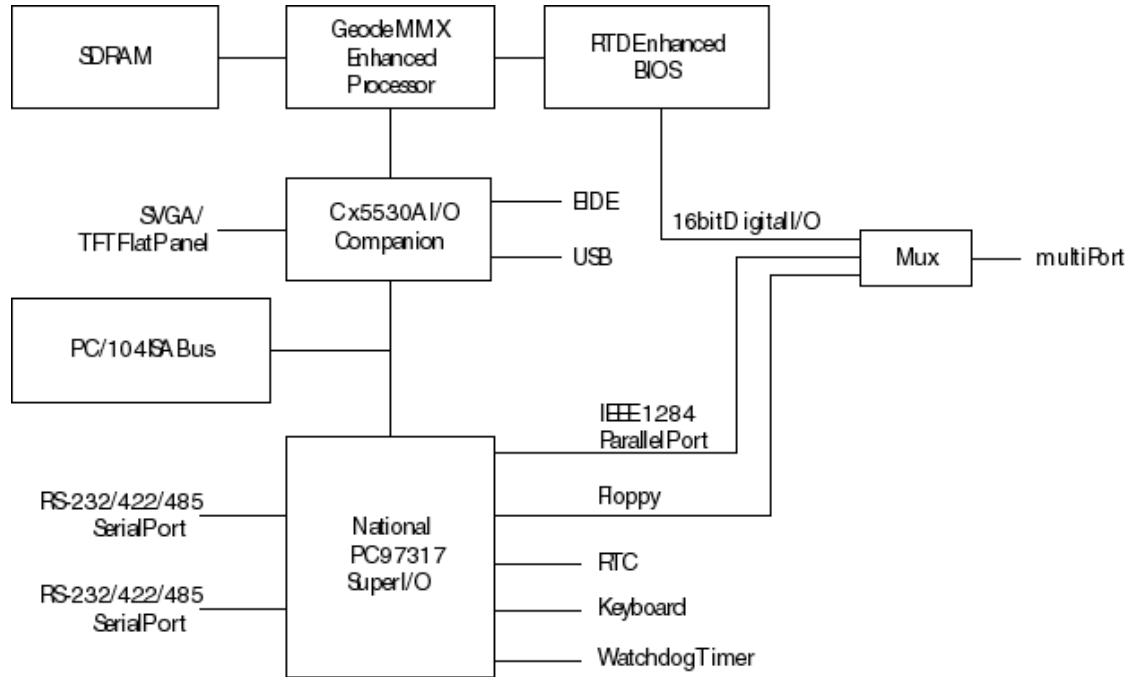


Figure 2 CMC26686CX cpuModule Simplified Block Diagram

You can easily customize the cpuModule by stacking PC/104 modules such as video controllers, modems, LAN controllers, or analog and digital data acquisition modules. Stacking PC/104 modules onto the cpuModule avoids expensive installations of backplanes and card cages, and preserves the module's compactness.

The cpuModule uses the RTD Enhanced Award BIOS. Drivers in the BIOS allow booting from floppy disk, hard disk, Solid State Disk (SSD), boot block flash, or ATA/IDE Disk Chip, thus enabling the system to be used with traditional disk drives or nonmechanical drives.

The cpuModule and BIOS are also compatible with most real-time operating systems for PC compatible computers, although these may require creation of custom drivers to use the SSD and watchdog timer.

Specifications

CMC26686CX300

- AMD Geode GX1 MMX enhanced microprocessor
- 300 MHz clock speed
- 2.0 V processor supply (provided onboard)
- 16 KB L1 cache
- Math coprocessor

CMC26686CX333

- AMD Geode GX1 MMX enhanced microprocessor
- 333 MHz clock speed
- 2.2 V processor supply (provided onboard)
- 16 KB L1 cache
- Math coprocessor

Memory Configurations

- 32 MB
- 128 MB
- 256 MB

Video Controller

- Analog SVGA monitor output supports:
 - 640 x 480 with 256 colors and 60, 72, 75, 85 Hz refresh
 - 640 x 480 with 65536 colors and 60, 72, 75, 85 Hz refresh
 - 800 x 600 with 256 colors and 60, 72, 75, 85 Hz refresh
 - 800 x 600 with 65536 colors and 60, 72, 75, 85 Hz refresh
 - 1024 x 768 with 256 colors and 60, 70, 75, 85 Hz refresh
 - 1024 x 768 with 65536 colors and 60, 70, 75, 85 Hz refresh
 - 1280 x 1024 with 256 colors and 60, 75, 85 Hz refresh
 - 1280 x 1024 with 65536 colors and 60, 75, 85 Hz refresh
- TFT flat panel output supports:
 - 640 x 480 with 256 colors and 60 Hz refresh
 - 640 x 480 with 65536 colors and 60 Hz refresh
 - 800 x 600 with 256 colors and 60 Hz refresh
 - 800 x 600 with 65536 colors and 60 Hz refresh
 - 1024 x 768 with 256 colors and 60 Hz refresh
 - 1024 x 768 with 65536 colors and 60 Hz refresh

DMA, Interrupts, Timers

- Seven (7) DMA channels (Intel 8237 compatible)
- Fifteen (15) interrupt channels (Intel 8259 compatible)
- Three (3) counter/timers (Intel 8254 compatible)

Advanced Digital I/O (aDIO™)

- Two 8-bit, TTL compatible, programmable Digital I/O ports
- One port is bit direction programmable and the other is byte direction programmable
- Advanced interrupt modes:
 - Interrupt on change
 - Interrupt on match
 - Interrupt on strobe

Table 2 aDIO DC Characteristics

Symbol	Parameter	Test Condition	Min.	Max.
V_{OH}	Output Voltage High	$I_{OH} = -4.0 \text{ mA}$	2.4 V	3.3 V
V_{OL}	Output Voltage Low	$I_{OL} = 8.0 \text{ mA}$	0.0 V	0.4 V
V_{IH}	Input Voltage High	—	2.0 V	5.5 V
V_{IL}	Input Voltage Low	—	0.0 V	0.8 V

Fail-Safe Boot ROM

- Surface-mount Flash chip that holds ROM-DOS™

ATA/IDE Disk Chip Socket

The cpuModule was designed to be used in embedded computing applications. In these applications, magnetic media like hard disks and floppy disks are not very desirable. It is possible to eliminate magnetic storage devices by placing your operating system and application software into the cpuModule's ATA/IDE Disk Chip socket.

Peripherals

- OneTwo serial ports software configurable for RS232/422/485; baud rates from 50 to 115200 baud in 16450 and 16550A compatible mode and 1.5 Mbaud in Extended UART mode
- Two USB 1.0 ports
- multiPort™, BIOS selectable as one of the following:
 - 16 bits of digital I/O (aDIO)
 - parallel port with SPP, ECP, EPP capability, and selectable interrupts and DMA channel
 - floppy drive controller
- UltraDMA EIDE Controller
- 32 pin ATA/IDE Disk Chip Socket
 - Miniature ATA/IDE Flash Disk Chip
 - Capacities up to 4GB¹
 - Natively supported by all major operating systems
- PC/AT standard keyboard port
- A PS/2 mouse port
- PC speaker port
- Real-time clock (requires user-supplied external battery for date and time backup)
- Watchdog timer with time-out of 1.2 seconds, typical

BIOS

- RTD Enhanced Award BIOS
- Directly supports ATA/IDE Disk Chip devices
- User-configurable using built-in Setup program
- Nonvolatile storage of CMOS settings
- Can boot from floppy disk, hard disk, SSD, or Fail Safe Boot ROM

Physical Characteristics

- Dimensions: 3.550 x 3.850 x 0.6 inches (90.2 x 97.8 x 15.2 mm)
- Weight: 4.16 ounces (120 grams)
- PCB: 14-layer, mixed surface-mount and thru-hole

Operating Environment

- Power supply: 5V ±5%
- 686GX1 processor operating temperature: –40 to +85°C case, with proper cooling (See *Processor Thermal Management* on page 82)
- Operating relative humidity: 0 to 90%, noncondensing
- Storage temperature : –55 to +125°C

1. During the time of this manual's publication, 4GB was the largest available ATA/IDE Disk Chip capacity

Power Consumption

Exact power consumption depends on the peripherals connected to the board, the selected SSD configuration, and the memory configuration. Table 3 lists power consumption for typical configurations and clock speeds.

Table 3 cpuModule Power Consumption

Module	Consumption, typ.	RAM	Disk Chip
CMC26686CX300 (300 MHz)	5.8 W	32, 128, or 256 MB	None
CMC26686CX333 (333 MHz)	6.3 W	32, 128, or 256 MB	None

Contact Information

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Chapter 2 Getting Started

For many users, the factory configuration of the CMC26686CX cpuModule can be used to get a PC/104 system operational. You can get your system up and running quickly by following the simple steps described in this chapter, which are:

1. Connect power.
2. Connect the utility cable.
3. Connect a keyboard.
4. Default BIOS configuration.
5. Fail Safe Boot ROM.
6. Connect a VGA monitor to the SVGA connector.

Refer to the remainder of this chapter for details on each of these steps.

Connector Locations

Figure 3 shows the connectors and the SSD socket of the CMC26686CX cpuModule.

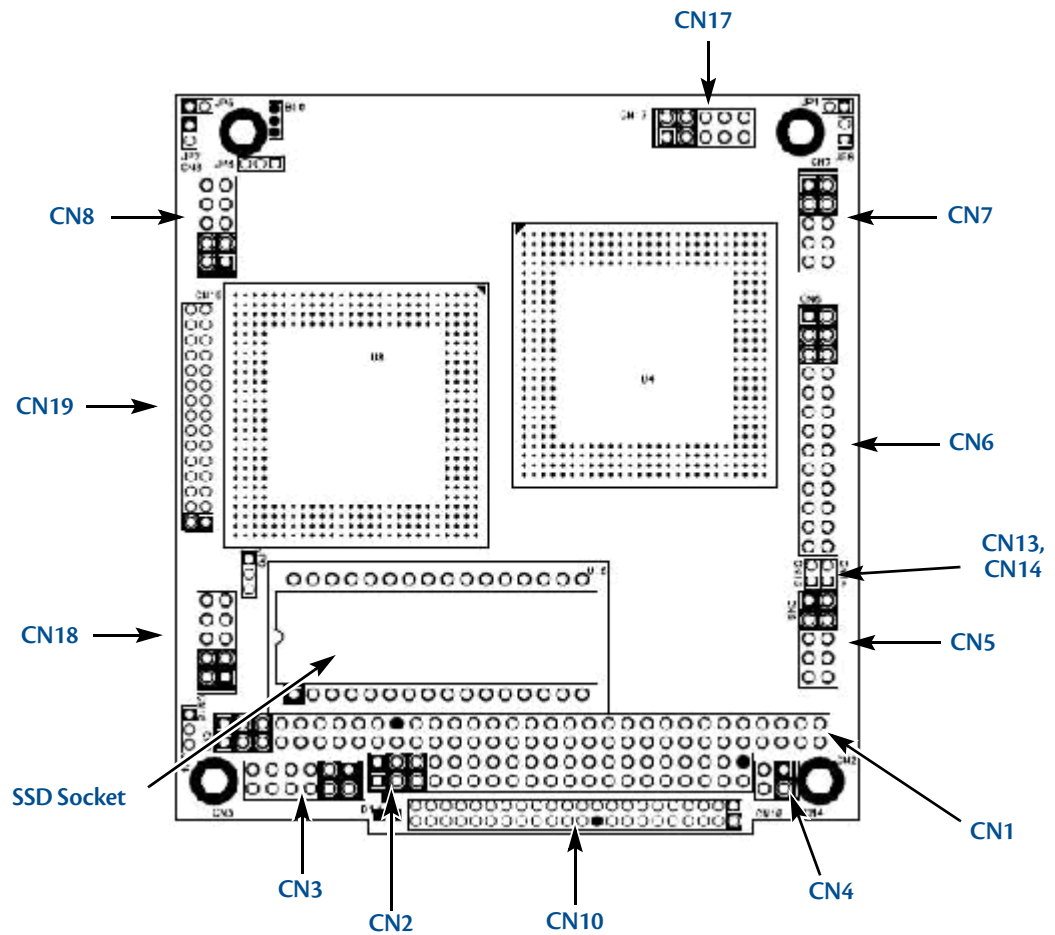


Figure 3 CMC26686CX Connector Locations



Note Pin 1 of each connector is indicated by a square within a white square on both the top and bottom of the board. Pin 1 of the XT, AT, and PCI connectors match when stacking cpuModules.

Table 4 CMC26686CX Basic Connectors

Connector	Function	Size
CN1	PC/104 Bus (XT)	64-pin
CN2	PC/104 Bus (AT)	40-pin
CN3	Auxiliary Power	12-pin
CN4	PS/2 Mouse	4-pin
CN5	Multi-Function	10-pin
CN6	multiPort	26-pin
CN7	Serial Port 1 (COM1)	10-pin
CN8	Serial Port 2 (COM2)	10-pin
CN10	EIDE Connector	44-pin
CN13	RTC Battery Input (optional)	2-pin
CN14	Fan Power (+5 V)	2-pin
CN17	USB	10-pin
CN18	Video (SVGA)	10-pin
CN19	Flat Panel Video	30-pin

Connecting Power



WARNING *If you connect power incorrectly, the module will almost certainly be damaged or destroyed. Such damage is not covered by the RTD warranty! Please verify connections to the module before applying power.*

Power is normally supplied to the cpuModule through the PC/104 bus connectors (**CN1** and **CN2**). If you are placing the cpuModule onto a PC/104 stack that has a power supply, you do not need to make additional connections to supply power.

If you are using the cpuModule without a PC/104 stack or with a stack that does not include a power supply, refer to on page 21 for more details.

Some PC/104-Plus expansion cards may require +3.3V supplied on the PC/104-Plus connector (**CN16**). In these cases, refer to on page 21 to learn how to supply this voltage.

Connecting the Utility Cable

The multi-function connector (**CN5**) implements the following interfaces:

- AT keyboard
- Speaker output
- System reset input
- Battery input

To use these interfaces, you must connect to the multi-function connector. If you are using the multi-function utility cable from the RTD cable kit, the cable provides a small speaker, a 5-pin circular DIN connector for the keyboard, a push-button for resetting the PC/104 system, and a lithium battery to provide backup power to the real time clock.

Refer to *Multi-Function Connector (CN5)* on page 29 to connect devices to the multi-function connector .

Connecting a Keyboard

You may plug a PC/AT compatible keyboard directly into the circular DIN connector of the multi-function cable in our cable kit.



Note *Some newer keyboards may use a smaller "mini-DIN" connector; you will need an adapter to plug these keyboards into the cpuModule. These connectors are available for order instead of the default circular DIN connector.*

Note *Many keyboards are switchable between PC/XT and AT operating modes, with the mode usually selected by a switch on the back or bottom of the keyboard. For correct operation with this cpuModule, you must select AT mode.*

Connecting to the PC/104 Bus

The PC/104 bus connectors of the cpuModule are simply plugged onto a PC/104 stack to connect to other devices.

RTD recommends that you follow the procedure below to ensure that stacking of the modules does not damage connectors or electronics.



WARNING Do not force the module onto the stack! Wiggling the module or applying too much pressure may damage it. If the module does not readily press into place, remove it, check for bent pins or out-of-place keying pins, and try again.

1. Turn off power to the PC/104 system or stack.
2. Select and install stand-offs to properly position the cpuModule on the PC/104 stack.
3. Touch a grounded metal part of the rack to discharge any buildup of static electricity.
4. Remove the cpuModule from its anti-static bag.
5. Check that keying pins in the bus connector are properly positioned.
6. Check the stacking order; make sure an XT bus card will not be placed between two AT bus cards or it will interrupt the AT bus signals.
7. Hold the cpuModule by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
8. Gently and evenly press the cpuModule onto the PC/104 stack.

Connecting to the PC/104-Plus PCI Bus

The cpuModule is simply plugged onto a PC/104 stack. Other PC/104-Plus boards may then connect to the cpuModule's PC/104-Plus bus connector. The cpuModule supplies power to the PCI bus.

To connect to the PC/104-Plus bus, follow the procedure described for connecting to the PC/104 bus.

There are three additional considerations when using the PCI bus:

- Slot selection switches on add-in boards
- PCI bus expansion card power
- PCI bus signaling levels

Slot Selection Switches

Unlike PC/104 cards, PC/104-Plus expansion cards have a "slot" selection switch or jumpers. In total, there are 4 PCI cards that can be stacked onto the cpuModule with switch positions 0 through 3. The distance from the CPU determines these switch settings. The card closest to the CPU is said to be in slot 0, the next closest slot 1 and so on to the final card as slot 3.



Note This requirement means that all PC/104-Plus cards must be stacked either on the top or the bottom of the CPU, not on both sides.

The "slot" setting method may vary from manufacturer to manufacturer, but the concept is the same. The CPU is designed to provide the correct delay to the clock signals to compensate for the bus length. The correct switch setting ensures the proper clock delay setting, interrupt assignment, and bus grant/request channel assignment. Refer to the expansion board's manual for the proper settings. Each expansion card must be in a different slot.

PCI Bus Expansion Card Power

+5 Volt DC

The +5 V power pins on the PC/104-Plus PCI bus are connected directly to the +5 V pins on the PC/104 connector and the power connector, **CN3** (pins 2 and 8).

+3.3 Volt DC

The factory-set default configuration is to connect the +3.3 V on the PCI bus to the auxiliary power connector (**CN3**) by soldering pins 2–3 on solder blob **B1** (See *Jumpers* — page 77). To use the onboard +3.3 V instead, change **B1** from pins 2–3 to pins 1–2.

PCI Bus Signaling Levels

The PCI bus can operate at +3.3 V or +5 V signaling levels. The signaling levels for the I/O pins on a PCI bus card are determined by solder blob **B3**. The default is +3.3 V. Refer to *Jumpers* — page 77 for solder blob settings.



WARNING You will have to ensure that all your expansion cards can operate together at a single signaling level.

Booting the CMC26686CX cpuModule for the First Time

You can now apply power to the cpuModule. You will see:

- A greeting message from the VGA BIOS (if the VGA BIOS has a sign-on message)
- The cpuModule BIOS version information
- A message requesting you press **Delete** to enter the Setup program

If you don't press **Delete**, the cpuModule will try to boot from the current settings. If you press **Delete**, the cpuModule will enter Setup. Once you have configured the cpuModule using Setup, save your changes and reboot.



Note You may miss the initial sign-on messages if your monitor takes a while to power on.

Note By default, cpuModules are shipped with Fail Safe Boot ROM enabled. When Fail Safe Boot ROM is enabled, the system will boot to it exclusively.

Default Configuration

In addition to the Setup configuration stored on the board, the CMC26686CX cpuModule has a permanent default configuration. The system will resort to using this default if an error occurs when accessing the BIOS Flash chip, which holds the Setup on the module. Refer to *Default Configuration* on page 17.

Booting to Boot Block Flash with Fail Safe Boot ROM

Fail Safe Boot ROM is supplied with the board. This feature is programmed into a surface-mount flash chip. The programmed boot ROM is ROM-DOS™. Fail Safe Boot ROM allows the system to boot without any attached storage devices, such as floppy, IDE, and SSD. Installing jumper **JPS** will force the cpuModule to use Fail Safe Boot ROM. This configuration allows you to boot to nonvolatile, onboard ROM-DOS™.



Note Boards are shipped with Fail Safe Boot ROM enabled. When Fail Safe Boot ROM is enabled, the system will boot to it exclusively.

The first time, your system will boot to the DOS prompt at the first available drive letter. If you do not intend to use REMSERV or REMDISK or if you intend to boot from another device, you will need to disable Fail Safe Boot ROM according to the procedure below.

1. Reset the system by either shutting it off and turning it on or by using the reset button.
2. While the system is booting, repeatedly press **Delete** to enter the BIOS setup.
3. Choose Integrated Peripherals using the arrow keys and press **Enter**.
4. Once in Integrated Peripherals set **Fail Safe Boot ROM** to **Disabled**.

If You Misconfigure the CMC26686CX cpuModule

It is possible that you may incorrectly configure the cpuModule using Setup. If this happens, the correct procedure is to:

1. Start rebooting the cpuModule.
2. While the system is rebooting, repeatedly press **Delete** until the cpuModule enters Setup.
3. Change the parameters to correctly match your system.

If this procedure fails:

1. Remove power from the system.
2. Install **JP5**.
3. Apply power to the system. The cpuModule will then boot to the Fail Safe image.
4. Run QBOOT.EXE, which will disable Quick Boot.
5. Reboot and press **Delete** to enter BIOS Setup.



Chapter 3 Connecting the cpuModule

This chapter provides information on all CMC26686CX cpuModule connectors.

Connector Locations — page 20

Auxiliary Power (CN3) — page 21

Serial Port 1 (CN7) Serial Port 1 (CN7) and Serial Port 2 (CN8) — page 23

multiPort™ (CN6) — page 26

Multi-Function Connector (CN5) — page 29

SVGA Video Connector (CN18) — page 31

Flat Panel Video Connector (CN19) — page 32

EIDE Connector (CN10) — page 33

ATA/IDE Disk Chip Socket (U16) — page 34

Bus Mouse Connector (CN4) — page 36

USB 1.0 Connector (CN17) — page 37

PC/104 Bus (CN1 and CN2) — page 38

PC/104-Plus PCI Bus (CN16) — page 41

Connector Locations

The figure below shows the connectors and the SSD socket of the CMC26686CX cpuModule.

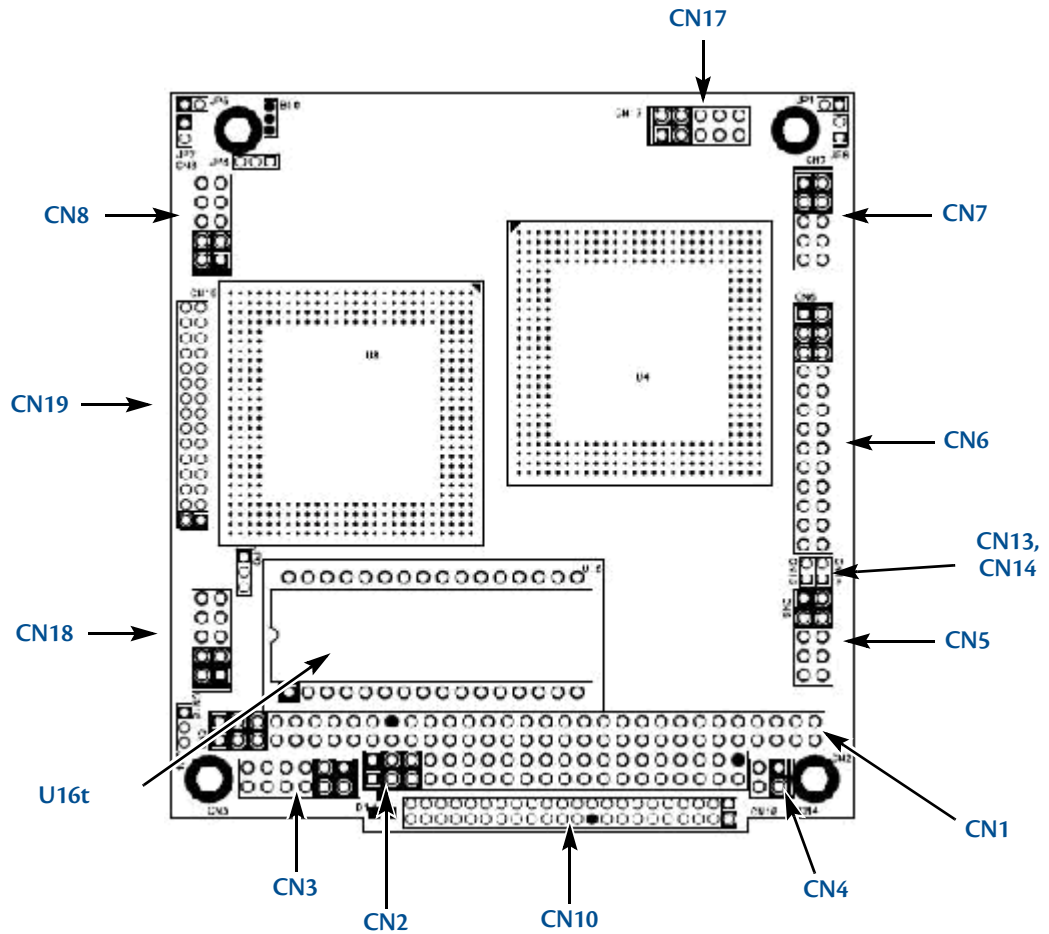


Figure 4 CMC26686CX Connector Locations



Note Pin 1 of each connector is indicated by a square within a white square on both the top and bottom of the board. Pin 1 of the XT, AT, and PCI connectors match when stacking cpuModules.

Table 5 CMC26686CX Basic Connectors

Connector	Function	Size
CN1	PC/104 Bus (XT)	64-pin
CN2	PC/104 Bus (AT)	40-pin
CN3	Auxiliary Power	12-pin
CN4	PS/2 Mouse	4-pin
CN5	Multi-Function	10-pin
CN6	multiPort	26-pin
CN7	Serial Port 1 (COM1)	10-pin
CN8	Serial Port 2 (COM2)	10-pin
CN10	EIDE Connector	44-pin
CN13	RTC Battery Input (optional)	2-pin
CN14	Fan Power (+5 V)	2-pin
CN17	USB	10-pin
CN18	Video (SVGA)	10-pin
CN19	Flat Panel Video	30-pin
U16	ATA/IDE Disk Chip socket	32-pin

Auxiliary Power (CN3)



WARNING *If you connect power incorrectly, the module will almost certainly be destroyed. Please verify power connections to the module before applying power.*

Power can be conveyed to the module either through the PC/104 bus (**CN1** and **CN2**) or through the Auxiliary Power connector (**CN3**). The cpuModule only requires +5 VDC and ground for operation; however, other modules in the system may require +12 VDC, -12 VDC, and -5 VDC. In these instances, the corresponding inputs on the Auxiliary Power Connector (**CN3**) may be used to supply these voltages.

Insufficient current supply will prevent your cpuModule from booting. The gauge and length of the wire used for connecting power to the cpuModule must be taken into consideration. Some power connectors have clip leads on them and may have significant resistance. Make sure that the input voltage does not drop below +4.8 V at the +5 V power pins. (Refer to Table 3 on page 9 for the cpuModule's power requirements). A good rule of thumb is to use wire that can supply twice the power required by the system.

Table 6 Auxiliary Power Connector (CN3)

Pin	Signal	Function
1	GND	Ground
2	+5 V	+5 Volts DC
3	N/C	Not Connected
4	+12 V	+12 Volts DC
5	-5 V	-5 Volts DC
6	-12 V	-12 Volts DC
7	GND	Ground
8	+5 V	+5 Volts DC
9	GND	Ground
10	+3.3 V	See note below
11	N/C	Not connected
12	+3.3 V	See note below



Note The +3.3 V pins (10 and 12) on the auxiliary power connector (**CN3**) are connected to the +3.3 V pins on the PC/104-Plus bus by default. They can be used to supply power to the PC/104-Plus bus, or to provide power to an external device. If +3.3 V is supplied to the PC/104-Plus connector from the onboard regulator, these pins are not connected. Refer to the **B1** description in the Appendix (see Jumpers — page 77).

Facing the connector pins, the pinout of the Auxiliary Power connector is:

11	9	7	5	3	1
N/C	GND	GND	-5 V	N/C	GND
+3.3 V	+3.3 V	+5 V	-12 V	+12 V	+5 V
12	10	8	6	4	2

Power Supply Protection

The cpuModule has protection circuitry that helps prevent damage due to problems with the +5 V supply, such as reversed polarity, overvoltage, and overcurrent.

Serial Port 1 (CN7) and Serial Port 2 (CN8)

Serial Port 1 (COM1) is implemented on connector **CN7**, and Serial Port 2 is implemented on connector **CN8**. The serial ports are normally configured as a PC compatible full-duplex RS-232 port, but you may use the Setup program to reconfigure these ports as half-duplex RS-422 or full-duplex RS-422 or RS-485. If you reconfigure the ports, you must also select the I/O address and corresponding interrupt using Setup. Table 7 provides the available I/O addresses and corresponding interrupts.

Table 7 Serial Port Settings

I/O Address (hex)	IRQ
03F8	IRQ4
02F8	IRQ3
03E8	IRQ4
02E8	IRQ3

Serial Port UART

The serial ports are implemented with a 16550-compatible UART (Universal Asynchronous Receiver/Transmitter). This UART is capable of baud rates up to 115.2 kbaud in 16450 and 16550A compatible mode and 1.5 Mbaud in Enhanced UART mode, and includes a 16-byte FIFO. Refer to any standard PC-AT hardware reference for the register map of the UART. For more information about programming UARTs, refer to the Appendix.

RS-232 Serial Port (Default)

The default serial port mode is full-duplex RS-232. With this mode enabled, the serial port connectors must be connected to an RS-232 compatible device. Table 8 provides the serial port connector pinout and shows how to connect to an external DB-25 or DB-9 compatible serial connector.

Table 8 Serial Port in RS-232 Mode

Pin	Signal	Function	In/Out	DB-25	DB-9
1	DCD	Data Carrier Detect	in	8	1
2	DSR	Data Set Ready	in	6	6
3	RXD	Receive Data	in	3	2
4	RTS	Request To Send	out	4	7
5	TXD	Transmit Data	out	2	3
6	CTS	Clear To Send	in	5	8
7	DTR	Data Terminal Ready	out	20	4
8	RI	Ring Indicate	in	22	9
9,10	GND	Signal Ground	—	7	5

Facing the serial port's connector pins, the pinout is:

9	7	5	3	1
GND	DTR	TXD	RXD	DCD
GND	RI	CTS	RTS	DSR
10	8	6	4	2

RS-422 or RS-485 Serial Port

You may use Setup to configure the serial portports as RS-422 or RS-485. In this case, you must connect the serial port to an RS-422 or RS-485 compatible device.

When using RS-422 or RS-485 mode, you can use the serial portports in either half-duplex (two-wire) or full-duplex (four-wire) configurations. For half-duplex (2-wire) operation, you must connect RXD+ to TXD+, and connect RXD- to TXD-.



Note The *cpuModule* has a 120 Ω termination resistor. Termination is usually necessary on all RS-422 receivers and at the ends of the RS-485 bus.

Note If required, the termination resistor can be enabled by closing jumper **JP1** for Serial Port 1 (COM1) or **JP2** for Serial Port 2 (COM2).

When using full-duplex (typically in RS-422 mode), connect the portports as shown in Table 9.

Table 9 Full-Duplex Connections

Port 1	Port 2
RXD+	TXD+
TXD+	RXD+
RXD-	TXD-
TXD-	RXD-

When using half-duplex in RS-485 mode, connect the portports as shown in Table 10.

Table 10 Half-Duplex RS-485 Mode

From	To
Port 1 TXD+	Port 1 RXD+
Port 1 TXD-	Port 1 RXD-
Port 1 TXD+	Port 2 RXD+
Port 1 RXD-	Port 2 TXD-

RS-422 and RS-485 Mode Pinout

Table 11 provides the serial port connector pinout when RS-422 or RS-485 modes are enabled.

Table 11 Serial Port in RS-422/485 Mode

Pin	Signal	Function	In/Out	DB-9
1	—	Data Carrier Detect	—	1
2	—	Data Set Ready	—	6
3	RXD-	Receive Data (-)	in	2
4	TXD+	Transmit Data (+)	out	7
5	TXD-	Transmit Data (-)	out	3
6	RXD+	Receive Data (+)	in	8
7	—	Reseved	—	4
8	—	Reseved	—	9
9,10	GND	Signal Ground	out	5

Facing the serial port connector, the pinout is:

9	7	5	3	1
GND	Rsvd	TXD-	RXD-	Rsvd
GND	Rsvd	RXD+	TXD+	Rsvd
10	8	6	4	2



Note When using the serial port in RS-485 mode, the serial transmitters are enabled and disabled under software control. The transmitters are enabled by manipulating the Request To Send (RTS*) signal of the serial port controller. This signal is controlled by writing bit 1 of the Modem Control Register (MCR) as follows:

- If MCR bit 1 = 1, then RTS* = 0, and serial transmitters are disabled
- If MCR bit 1 = 0, then RTS* = 1, and serial transmitters are enabled

Note For more information on the serial port registers, including the MCR, refer to the Appendix.

multiPort™ (CN6)

RTD's exclusive multiPort can be configured as an Advanced Digital I/O (aDIO™), a parallel port, or a floppy drive. Refer to Chapter 4, *Configuring the cpuModule (BIOS Setup)*, to configure the multiPort.

multiPort Configured as an Advanced Digital I/O (aDIO™) Port

The multiPort connector (CN6) can be configured as an aDIO port. aDIO is 16 digital bits configured as 8-bit programmable and 8-bit port programmable I/O, providing any combination of inputs and outputs. Match, event, and strobe interrupt modes mean no more wasting valuable processor time polling digital inputs. Interrupts are generated when the 8-bit programmable digital inputs match a pattern, or on any value change event. Bit masking allows selecting any subgroup of 8 bits. The strobe input latches data into the bit programmable port and generates an interrupt. Refer to *Advanced Digital I/O Ports (aDIO™)* on page 68 for information on programming the multiPort.

Table 12 multiPort aDIO Pinout

CN6 Pin	Function	CN6 Pin	Function
1	strobe 0	2	P0-4
3	P1-0	4	P0-5
5	P1-1	6	P0-6
7	P1-2	8	P0-7
9	P1-3	10	strobe 1
11	P1-4	12	GND
13	P1-5	14	GND
15	P1-6	16	GND
17	P1-7	18	GND
19	P0-0	20	GND
21	P0-1	22	GND
23	P0-2	24	GND
25	P0-3	26	+5 V

multiPort Configured as a Parallel Port

The parallel port is available on connector **CN6**. Make sure the BIOS Setup sets the multiPort to parallel port. You can use the BIOS Setup to select the parallel port's address and associated interrupt, and choose between its operational modes (SPP, ECP, EPP 1.7, and EPP 1.9).

The pinout of the connector enables a ribbon cable to be connected directly to a DB-25 connector, thus providing a standard PC compatible port.



Note For correct operation, keep the length of the cable connecting the cpuModule and parallel device less than 3 meters (10 feet).

Table 13 lists the parallel port signals and explains how to connect it to a DB-25 connector to obtain a PC compatible port.

Table 13 multiPort Connector (CN6) as a Parallel Port

CN6 Pin	Signal	Function	In/Out	DB-25
1	STB	Strobe Data	out	1
2	AFD	Autofeed	out	14
3	PD0	Printer Data 0 (LSB)	out	2
4	ERR	Printer Error	in	15
5	PD1	Parallel Data 1	out	3
6	INIT	Initialize Printer	out	16
7	PD2	Printer Data 2	out	4
8	SLIN	Select Printer	out	17
9	PD3	Printer Data 3	out	5
10	GND	Signal Ground	—	18
11	PD4	Printer Data 4	out	6
12	GND	Signal Ground	—	19
13	PD5	Printer Data 5	out	7
14	GND	Signal Ground	—	20
15	PD6	Printer Data 6	out	8
16	GND	Signal Ground	—	21
17	PD7	Printer Data 7 (MSB)	out	9
18	GND	Signal Ground	—	22
19	ACK	Acknowledge	in	10
20	GND	Signal Ground	—	23
21	BSY	Busy	in	11
22	GND	Signal Ground	—	24
23	PE	Paper End	in	12
24	GND	Signal Ground	—	25
25	SLCT	Ready To Receive	in	13
26	—	+5 V	—	—

multiPort Configured as a Floppy Drive Controller

The multiPort (**CN6**) can be configured to be a floppy drive controller. This is selected in the BIOS Setup under Integrated Peripherals. Only one floppy drive can be connected to the multiPort, and it is configured as the second drive.



Note To boot the CPU from the multiPort Floppy as drive **A**, apply the following settings to the system. A hardware reset (power off/on) is required to enable these changes.

- With the system powered off, attach a floppy drive with an adapter board to **CN6**.
- Power on the system and enter the BIOS setup screen by pressing the delete key as the system boots.
- Set Drive B to **1.44 MB** in the Standard CMOS Settings section of BIOS Setup.
- Set Swap Floppy Drive to **Enabled** in the BIOS Features Setup section of BIOS Setup.
- Set the first boot device in the Boot Sequence to Drive **A**: in the BIOS Features Setup section of BIOS Setup.
- Set the multiPort to **Floppy** in the Integrated Peripherals section of BIOS Setup.
- Set mapping of Drive **A**: to **Floppy** in the Integrated Peripherals section of BIOS Setup.

Table 14 shows the pin assignments to connect a floppy drive to the multiPort.

Table 14 multiPort Connector Floppy Pinout (CN6)¹

CN6 Pin	Function	DB-25	Floppy Drive Pin
1	DS0#	1	14
2	DR0	14	2
3	INDEX#	2	8 ²
4	HDSEL#	15	32
5	TRK0#	3	26 ²
6	DIR#	16	18
7	WRTprt#	4	28 ²
8	STEP#	17	20
9	RDATA#	5	30 ²
10	GND	18	—
11	DSKCHG	6	34 ²
12	GND	19	odd pins
13	—	7	—
14	GND	20	odd pins
15	MTR0#	8	10
16	GND	21	odd pins
17	—	9	—
18	GND	22	odd pins
19	DS1#	10	12
20	GND	23	odd pins
21	MTR1#	11	16
22	GND	24	odd pins
23	WDATA#	12	22
24	GND	25	odd pins
25	WGATE#	13	24
26	+5 V	—	—

1. Signals marked with (#) are active low.
2. These signals are pulled up to +5 V on the board.

Multi-Function Connector (CN5)

The multi-function connector implements the following functions:

- Speaker output
- AT keyboard
- System reset input
- Battery Input

Table 15 provides the pinout of the multi-function connector.

Table 15 Multifunction Connector (CN5)

Pin	Signal	Function	In/Out
1	SPKR+	Speaker Output (open collector)	out
2	PWR	+5 V	out
3	RESET	Manual Push-Button Reset	in
4	—	Not Connected	—
5	KBD	Keyboard Data	in
6	KBC	Keyboard Clock	out
7	GND	Ground	—
8	PWR	+5 V	out
9	BAT	Battery input	in
10	—	Not Connected	—

Facing the connector pins, the pinout is:

9	7	5	3	1
BAT	GND	KBD	RESET	SPKR+
—	PWR	KBC	—	PWR
10	8	6	4	2

Speaker

A speaker output is available on pins 1 and 2 of the multi-function connector. These outputs are controlled by a transistor to supply 0.1 W of power to an external speaker. The external speaker should have 8 Ω impedance and be connected between pins 1 and 2.

Keyboard

An AT compatible keyboard can be connected to the multi-function connector. Usually PC keyboards come with a cable ending with a 5-pin male DIN connector. Table 16 lists the relationship between the multi-function connector pins and a standard DIN keyboard connector.

Table 16 Keyboard Connector Pins (CN5)

Pin	Signal	Function	DIN
5	KBD	Keyboard Data	2
6	KBC	Keyboard Clock	1
7	GND	Ground	4
8	KBP	Keyboard Power (+5 V)	5

To ensure correct operation, check that the keyboard is either an AT compatible keyboard or a switchable XT/AT keyboard set to AT mode. Switchable keyboards are usually set by a switch on the back or bottom of the keyboard.

System Reset

Pin 3 of the multi-function connector allows connection of an external push-button to manually reset the system. The push-button should be normally open, and connect to ground when pushed.

Battery

Pin 9 of the multi-function connector is the connection for an external backup battery (in the range of 2.40 V to 3.7 V; typically 3.0 or 3.6 V). This battery is used by the cpuModule when system power is removed in order to preserve the date and time of the real time clock.

SVGA Video Connector (CN18)

Table 17 provides the pinout of the video connector.

Table 17 SVGA Video Connector (CN18)

Pin	Signal	Function	In/Out
1	VSYNC	Vertical Sync	out
2	HSYNC	Horizontal Sync	out
3	DDCSCL	Monitor Communications Clock	out
4	RED	Red Analog Output	out
5	DDCSDA	Monitor Communications Data	bidirectional
6	GREEN	Green Analog Output	out
7	PWR	+5 V	out
8	BLUE	Blue Analog Output	out
9	GND	Ground	out
10	GND	Ground	out

Facing the connector pins of the SVGA Video connector (**CN18**), the pinout is:

9	7	5	3	1
GND	N/C	DDCSDA	DDCSCL	VSYNC
GND	BLUE	GREEN	RED	HSYNC
10	8	6	4	2

Refer to Chapter 4, *Configuring the cpuModule (BIOS Setup)*, for supported video resolutions and BIOS settings.

Flat Panel Video Connector (CN19)

The CMC26686CX cpuModule supports a variety of flat panels. Supported flat panels include NEC model number NL6448AC20 and Optrex model number T-51512D121J-FW-A-AB. Table 18 provides the pinout of the Flat Panel Video connector (**CN19**). FP_VCC can be either +5 V or +3.3 V, and is selected with jumper **JP8**. FP_VBKLT can be either +5 V or +12 V, and can be selected with **JP9**. See *Jumpers* on page 77 for more details.

Table 18 Flat Panel Video Connector (CN19)

Pin	Signal	Function	In/Out
1	FP_VCC	Power for Flat Panel Electronics	out
2	FP_VBKLT	Power for Flat Panel Backlight	out
3	FP_VDDEN	Enable for Flat Panel Power	out
4	FP_ENABLK	Enable for Backlight Power	out
5	GND	Ground	GND
6	FP_DISPEN	Display Enable	out
7	GND	Ground	GND
8	FP_HSYNC	Horizontal Sync	out
9	FP_VSYNC	Vertical Sync	out
10	GND	Ground	GND
11	FP_CLK	Clock	out
12	GND	Ground	GND
13	FP_BLUE0	Blue Bit 0 (LSB)	out
14	FP_BLUE1	Blue Bit 1	out
15	FP_BLUE2	Blue Bit 2	out
16	FP_BLUE3	Blue Bit 3	out
17	FP_BLUE4	Blue Bit 4	out
18	FP_BLUE5	Blue Bit 5 (MSB)	out
19	FP_GREEN0	Green Bit 0 (LSB)	out
20	FP_GREEN1	Green Bit 1	out
21	FP_GREEN2	Green Bit 2	out
22	FP_GREEN3	Green Bit 3	out
23	FP_GREEN4	Green Bit 4	out
24	FP_GREEN5	Green Bit 5 (MSB)	out
25	FP_RED0	Red Bit 0 (LSB)	out
26	FP_RED1	Red Bit 1	out
27	FP_RED2	Red Bit 2	out
28	FP_RED3	Red bit 3	out
29	FP_RED4	Red Bit 4	out
30	FP_RED5	Red Bit 5 (MSB)	out

EIDE Connector (CN10)

The EIDE connector is a 44-pin, 2 mm connector that can connect to a variety of EIDE or IDE devices. The connector provides all signals and power needed to use a 2.5-inch form factor (laptop) hard drive. Also, the first 40 pins of the connector provide all of the signals needed to interface to a 3.5-inch or 5-inch form factor hard drive, CD-ROM drive, or other EIDE device. The larger form factors use a 40-pin, 0.1 inch spacing connector, so an adapter cable or adapter board is needed.

Table 19 EIDE Connector (CN10)¹

Pin	Signal	Pin	Signal
1	RESET#	2	Ground
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	Ground	20	N/C
21	DMARQ	22	Ground
23	DIOW#:STOP	24	Ground
25	DIOR#:HDMARDY#:HSTROBE	26	Ground
27	IORDY:DDMARDY#:DSTROB	28	CSEL
29	DMACK#	30	Ground
31	INTRQ	32	N/C
33	DA1	34	PDIAGDA0
35	N/C	36	DA2
37	CS0#	38	CS1#
39	DASP#	40	Ground
41	+5 V (logic)	42	+5 V (motor)
43	Ground	44	N/C

1. Signals marked with (#) are active low.

ATA/IDE Disk Chip Socket (U16)

The ATA/IDE Disk Chip socket is a 32-pin socket that supports +3.3V or +5V miniature ATA/IDE flash disk chips. The socket allows a true IDE device to be attached to the board with either a socketed or soldered connection. Such true IDE devices are supported by all major operating systems, and do not require special drivers.



WARNING The ATA/IDE Disk Chip socket does not support conventional SSD memory devices or devices that install as a BIOS extension (such as the M-Systems DiskOnChip®). If such a device is installed, the cpuModule and device will almost certainly be destroyed.

Table 20 ATA/IDE Disk Chip Socket (U16)¹

Pin	Signal	Pin	Signal
1	RESET#	32	VDD ²
2	D7	31	D8
3	D6	30	D9
4	D5	29	D10
5	D4	28	D11
6	D3	27	D12
7	D2	26	D13
8	D1	25	D14
9	D0	24	D15
10	DMARQ/WP#	23	IOWR#
11	IORD#	22	DMACK/CSEL
12	INTRQ	21	IOCS16#
13	A1	20	PDIAG#
14	A0	19	A2
15	CS1FX#	18	CS3FX#
16	GND	17	DASP#

1. Signals marked with (#) are active low.
2. VDD may be set to +3.3 V or +5 V with jumper **JP4**

Installing and Configuring the ATA/IDE Disk Chip

To ensure proper installation and of the ATA/IDE Disk Chip, follow the following configuration steps. Note that the first few steps must be performed **before installing the Disk Chip**.

1. Before installing the ATA/IDE Disk Chip in the Disk Chip Socket (**U16**), specify the Disk Chip supply voltage by setting jumper **JP4** to select either +3.3V or +5V. Refer to *Jumpers* on page 77 for more details.
2. Next, apply power to the system, and press the delete key repeatedly to enter the BIOS setup screen. Once in the BIOS, specify the following settings:
 - a. Enable the cpuModule's secondary IDE channel.
 - b. Specify the IDE mode of the ATA/IDE Disk Chip. For more information on the supported IDE modes, refer to to *Configuring the ATA/IDE Disk Chip Socket* section of this manual on page 76.
 - c. Save the settings in the BIOS setup

3. Remove power from the system.



WARNING *The preceding steps should be performed before installing the Disk Chip in the ATA/IDE Disk Chip Socket. These steps ensure that the system is properly configured for the correct device and supply voltage, so neither the Disk Chip or cpuModule are damaged.*

4. Insert the Disk Chip in the ATA/IDE Disk Chip Socket (**U16**) aligning pin 1 with the square solder pad on the board.
5. Apply power to the system.
6. Re-enter the BIOS and set the boot order of the system accordingly.

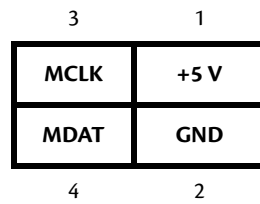
Bus Mouse Connector (CN4)

Table 21 provides the pinout of the Bus Mouse connector (CN4).

Table 21 Bus Mouse Connector (CN4)

Pin	Signal	Function	In/Out
1	+5 V	+5 Volts	out
2	GND	Ground	out
3	MCLK	Mouse Clock	out
4	MDAT	Mouse Data	bidirectional

Facing the connector pins, the pinout is:



USB 1.0 Connector (CN17)

Two USB 1.0 compliant connector are available on connector, **CN17**. Table 22 provides the pinout of the USB connector.

Table 22 USB Mouse Connector (CN17)

Pin	Signal	Function	In/Out
1	VCC1	Supply +5 V to USB1	out
2	VCC2	Supply +5 V to USB2	out
3	DATA1-	Bidirectional data line for USB1	in/out
4	DATA2-	Bidirectional data line for USB2	in/out
5	DATA1+	Bidirectional data line for USB1	in/out
6	DATA2+	Bidirectional data line for USB2	in/out
7	GND	Ground	out
8	GND	Ground	out
9	GND	Ground	out
10	GND	Ground	out

Facing the connector pins, the pinout is:

9	7	5	3	1
GND	GND	DATA1+	DATA1-	VCC1
GND	GND	DATA2+	DATA2-	VCC2
10	8	6	4	2

PC/104 Bus (CN1 and CN2)

Connectors **CN1** and **CN2** carry signals of the PC/104 bus; these signals match definitions of the IEEE P996 standard. Table 23 list the pinouts of the PC/104 bus connectors, with the CMC26686CX cpuModule oriented with the PC/104 bus at the nine o' clock position (toward the left).

Table 23 PC/104 (ISA) Bus Connectors (AT and XT Connectors)¹

			CN1		
			Pin	Row A	Row B
			1	IOCHK#	GND
			2	SD7	RESET
			3	SD6	+5 V
			4	SD5	IRQ9
			5	SD4	-5 V
			6	SD3	DRQ2
			7	SD2	-12 V
			8	SD1	SRDY#
Pin	CN2		9	SD0	+12 V
0	GND	GND	10	IOCHRDY	KEY
1	MEMCS16#	SBHE#	11	AEN	SMEMW#
2	IOCS16#	LA23	12	SA19	SMEMR#
3	IRQ10	LA22	13	SA18	IOW#
4	IRQ11	LA21	14	SA17	IOR#
5	IRQ12	LA20	15	SA16	DACK3#
6	IRQ15	LA19	16	SA15	DRQ3
7	IRQ14	LA18	17	SA14	DACK1#
8	DACK0#	LA17	18	SA13	DRQ1
9	DRQ0	MEMR#	19	SA12	REFRESH#
10	DACK5#	MEMW#	20	SA11	BCLK
11	DRQ5	SD8	21	SA10	IRQ7
12	DACK6#	SD9	22	SA9	IRQ6
13	DRQ6	SD10	23	SA8	IRQ5
14	DACK7#	SD11	24	SA7	IRQ4
15	DRQ7	SD12	25	SA6	IRQ3
16	+5 V	SD13	26	SA5	DACK2#
17	MASTER#	SD14	27	SA4	TC
18	GND	SD15	28	SA3	BALE
19	GND	KEY	29	SA2	+5 V
			30	SA1	OSC
			31	SA0	GND
			32	GND	GND

¹Signals marked with (#) are active low.



Note This cpuModule does not support ISA masters or ISA bus refresh.

Note Keying pin positions have the pin cut on the bottom of the board and the hole plugged in the connector to prevent misalignment of stacked modules. This is a feature of the PC/104 specification and should be implemented on all mating PC/104 modules.

Note All bus lines can drive a maximum current of 4 mA at TTL voltage levels.

PC/104 Bus Signals

Table 24 provides brief descriptions of the PC/104 bus signals.

Table 24 PC/104 Bus Signals¹

Signal	I/O	Description
AEN	O	Address Enable: when this line is active (high), it means a DMA transfer is being performed, and therefore, the DMA controller has control over the data bus, the address bus, and the control lines.
BALE	O	Bus Address Latch Enable, active high. When active, it indicates that address lines SA0 to SA19 are valid.
DACKx#	O	DMA ACKnowledge x=0 to 7, active low, used to acknowledge DMA requests.
DRQx	I	DMA Request x=0 to 7: these are asynchronous lines used by peripheral devices to request DMA service. They have increasing priority from DRQ0 up to DRQ7. A DMA request is performed by setting the DRQ line high and keeping it high until the corresponding DACK line is activated.
ENDXFR#	I/O	This is the only synchronous signal of the PC/104 bus and it is active low. It indicates that the current bus cycle must be performed with 0 wait states. It is used only for 16-bit boards.
IOCHCHK#	I	I/O Channel Check, active low, indicates an error condition that cannot be corrected.
IOCHRDY	I	I/O Channel Ready: this line, usually high (ready) is pulled to a low level by devices which need longer bus cycles.
IOCS16#	I	I/O Chip Select 16-bit: this line, active low, is controlled by devices mapped in the I/O address space. It indicates they have a 16-bit bus width.
IOR#	O	I/O Read, active low, indicates when the devices present on the bus can send their information on the data bus.
IOW#	O	I/O Write, active low. When active, it allows the peripheral devices to read data present on the data bus.
IRQx	I	Interrupt Request: x = 2 to 15, active on rising edge. IRQ15 has top priority; the other lines have decreasing priority starting from IRQ14 down to IRQ2. An interrupt request is performed by changing the level of the corresponding line from low to high and keeping it high until the microprocessor has recognized it.
KEY	—	These locations contain mechanical keying pins to help prevent incorrect connector insertion.
LA23..LA17	O	These signals select a 128 KB window in the 16 MB address space available on the bus.
MASTER#	I	During a DMA cycle, this active-low signal, indicates that a resource on the bus is about to drive the data and address lines.
MEMCS16#	I	Memory Chip Select 16-bit: this line, active low, is controlled by devices mapped in the memory address space and indicates they have a 16-bit bus width.
MEMR#	I/O	This active-low signal indicates a memory read operation. Devices using this signal must decode the address on lines LA23..LA17 and SA19..SA0.
MEMW#	I/O	This active-low signal indicates a memory write operation. Devices using this signal must decode the address on lines LA23..LA17 and SA19..SA0.
OSC	O	OSCillator: clock with a 70 ns period and a 50% duty cycle. It is a 14.31818 MHz always presents.
REFRESH#	I	This cpuModule does not support refresh on the ISA bus. This pin is pulled high with a 4.7 kΩ resistor and may be driven by another card in the PC/104 stack.

Table 24 PC/104 Bus Signals¹ (cont'd)

Signal	I/O	Description
RESETDRV	O	This line, active high, is used to reset the devices on the bus, at power-on or after a reset command.
SA0..19	O	Address bits 0 to 19: these lines are used to address the memory space and the I/O space. SA0 is the least significant bit while SA19 is the most significant bit.
SBHE#	O	This active-low signal indicates a transfer of the most significant data byte (SD15..SD8).
SD8..15	I/O	Data bits: these are the high-byte data bus lines. SD8 is the least significant bit; SD15 the most significant bit.
SD0..7	I/O	Data bits: these are the low-byte data bus lines. SD0 is the least significant bit; SD7 the most significant bit.
SMEMR#	O	Memory Read command, active low.
SMEMW#	O	Memory Write command, active low.
SYCLK	O	System Clock, 8.0 MHz with a 50% duty cycle. Only driven during external bus cycles.
TC	O	Terminal Count: this line is active high and indicates the conclusion of a DMA transfer.

1. Signals marked with (#) are active low.

PC/104 Bus Termination

Termination of PC/104 bus signals is not recommended since this cpuModule incorporates source termination on bus signals. Additional termination is unnecessary and may cause the cpuModule to malfunction.

PC/104-Plus PCI Bus (CN16)

Connector **CN16** carries the signals of the PC/104-Plus PCI bus. These signals match definitions of the PCI Local Bus specification Revision 2.1. Table 25 list the pinouts of the PC/104-Plus bus connector.

Table 25 PC/104-Plus Bus Signal Assignments¹

Pin	A	B	C	D
1	GND	Reserved	+5 V	AD00
2	VIO	AD02	AD01	+5 V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VIO	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3 V	C/BE1#	AD15	+3.3 V
9	SERR#	GND	Reserved	PAR
10	GND	PERR#	+3.3 V	Reserved
11	STOP#	+3.3 V	LOCK#	GND
12	+3.3 V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3 V
14	GND	AD16	+3.3 V	C/BE2#
15	AD18	+3.3 V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3 V	AD23	AD22	+3.3 V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VIO	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5 V	AD28	AD27
22	+5 V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VIO
24	GND	REQ2#	+5 V	GNT0#
25	GNT1#	VIO	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5 V	CLK3	GND
28	GND	INTD#	+5 V	RST#
29	+12 V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND

1. Signals marked with (#) are active low.

PC/104-Plus PCI Bus Signals

The following are brief descriptions of the PC/104-Plus PCI bus signals.

Address and Data

AD[31:00] — Address and Data are multiplexed. A bus transaction consists of an address cycle followed by one or more data cycles.

C/BE[3:0]# — Bus Command/Byte Enables are multiplexed. During the address cycle, the command is defined. During the Data cycle, they define the byte enables.

PAR — Parity is even on AD[31:00] and C/BE[3:0]# and is required.

Interface Control Pins

FRAME# — Frame is driven by the current master to indicate the start of a transaction and will remain active until the final data cycle.

TRDY# — Target Ready indicates the selected device's ability to complete the current data cycle of the transaction. Both IRDY# and TRDY# must be asserted to terminate a data cycle.

IRDY# — Initiator Ready indicates the master's ability to complete the current data cycle of the transaction.

STOP# — Stop indicates the current selected device is requesting the master to stop the current transaction.

DEVSEL# — Device Select is driven by the target device when its address is decoded.

IDSEL[3:0] — Initialization Device Select is used as a chip-select during configuration.

LOCK# — Lock indicates an operation that may require multiple transactions to complete.

Error Reporting

PERR# — Parity Error is for reporting data parity errors.

SERR# — System Error is for reporting address parity errors.

Arbitration (Bus Masters Only)

REQ[3:0]# — Request indicates to the arbitrator that this device desires use of the bus.

GNT[3:0]# — Grant indicates to the requesting device that access has been granted.

System

CLK — Clock provides timing for all transactions on the PCI bus.

RST# — Reset is used to bring PCI-specific registers to a known state.

Interrupts

INTA# — Interrupt A is used to request Interrupts.

INTB# — Interrupt B is used to request Interrupts only for multi-function devices.

INTC# — Interrupt C is used to request Interrupts only for multi-function devices.

INTD# — Interrupt D is used to request Interrupts only for multi-function devices.

Power Supplies and VIO

+5 V — +5 V supply connected to PC/104 bus and auxiliary power connector (**CN3**) +5 V supplies.

+12 V — +12 V supply connected to PC/104 bus and auxiliary power connector (**CN3**) +12 V supplies.

-12 V — -12 V supply connected to PC/104 bus and auxiliary power connector (**CN3**) -12 V supplies.

+3.3 V — +3.3 V supply is an onboard converter which can deliver up to 2 A.

VIO — This signal is typically the I/O power to the bus drivers on a PCI bus card. Signaling level is determined by solder blob **B3**. The default is +3.3 V. Refer to the Appendix (see *Jumpers* — page 77) for solder blob settings.



Chapter 4 Configuring the cpuModule (BIOS Setup)

This chapter contains information to configure the CMC26686CX cpuModule.

Entering the BIOS Setup — page 46

If You Are Unable to Enter BIOS Setup — page 46

Booting to Boot Block Flash with Fail Safe Boot ROM — page 46

Disabling Fail Safe Boot ROM — page 47

Quick Boot — page 47

Configuring with the RTD Enhanced Award BIOS — page 48

Supported Video Resolutions and BIOS Settings — page 60

Entering the BIOS Setup

1. Apply power to the system.
2. Repeatedly press **Delete** key to enter Setup.

If You Are Unable to Enter BIOS Setup

There are some configurations with Quick Boot enabled in which the cpuModule boots so quickly that it is very difficult to enter BIOS Setup. In these situations, follow the procedure below.

1. Remove power from the system.
2. Install **JP5**.
3. Apply power to the system. The cpuModule will then boot to the Fail Safe image.
4. Run QBOOT.EXE, which will disable Quick Boot.
5. Reboot and press **Delete** to enter BIOS Setup.

Booting to Boot Block Flash with Fail Safe Boot ROM



Note Boards are shipped with Fail Safe Boot ROM enabled. When Fail Safe Boot ROM is enabled, the system will boot to it exclusively.

The Fail Safe Boot ROM is a special build of ROM-DOS™ located inside a surface-mounted Boot Block Flash chip that is memory mapped to the SSD window. Boot Block Flash is a write-protected flash device that contains the BIOS and extra room where the Fail Safe Boot ROM is stored. The ROM-DOS build is special because it can understand the format of the flash chip. Additionally, Fail Safe Boot ROM is an emergency interface accessible by an external computer. The ROM DISK contains REMDISK and REMSERVE for remote access to the system's disk drives. Due to the size of the flash chip, Fail Safe Boot ROM contains an abbreviated selection of the ROM-DOS™ utilities; however, the complete ROM-DOS™ is contained on a CD shipped with the cpuModule.

The purpose of the Fail Safe Boot ROM is to make the cpuModule bootable upon receipt. Fail Safe Boot ROM can be used as an indicator of the module's functionality when booting problems arise with another operating system. This test can be accomplished by installing **JP5**. Installing this jumper forces the cpuModule to boot to Fail Safe Boot ROM. The ROM DISK that contains the Fail Safe Boot ROM acts as an example of what can be programmed into the flash chip. Finally, Fail Safe Boot ROM allows files to be transferred on or off the storage devices in the system by use of the two ROM-DOS™ utilities, REMSERV and REMDISK .

If you need remote access to the system, run REMSERV on the target system and REMDISK on the host system. The end result would be that the storage devices on the target system would appear as additional drives on the host system. Information could then be transferred between hard disks by using a standard NULL Modem cable over a serial port. REMSERV makes the connection appear as an additional drive to the user. For details concerning this type of access, please refer to the ROM-DOS™ user's guide shipped with your board.

Disabling Fail Safe Boot ROM

The first time, your system will boot to the DOS prompt at the first available drive letter. If you do not intend to use REMSERV or REMDISK or if you intend to boot from another device, you will need to disable Fail Safe Boot ROM according to the procedure below.

1. Reset the system by either shutting it off and turning it on or by using the reset button.
2. While the system is booting, repeatedly press **Delete** to enter the BIOS setup.
3. Choose Integrated Peripherals using the arrow keys and press **Enter**.
4. Once in Integrated Peripherals set **Fail Safe Boot** to **Disabled**.

Quick Boot

The BIOS contains a Quick Boot option that minimizes the boot time of the system. Quick Boot eliminates the exhaustive tests that are performed during Power On Self Test (POST) while maintaining the functionality of the board (see note 1 below). By enabling the Quick Boot feature, your system can achieve 5-second boot times as shown below.

Table 26 BIOS Settings and Boot Times

		Normal Boot	Quick Boot
Standard RTD Defaults		~ 16 seconds	< 10 seconds
Primary Master:	None	~ 20 seconds	< 6 seconds
Primary Slave:	None		
Secondary Master:	None		
Secondary Slave:	None		
Same as above including, ISA Plug-n-Play Support:	Disabled	~ 18 seconds	< 5 seconds

To achieve boot times of 6 seconds or less, you will have to disable the HDD and possibly any other devices attached to the IDE controller.

To achieve boot times of 5 seconds or less, ISA Plug-n-Play Support must be disabled. If there is not an ISA PnP card attached to your system, then disabling this feature will save at least 1 second. Some modern operating systems (Windows) will automatically configure ISA PnP devices. If using one of these operating systems, ISA Plug-n-Play cards will still work even if disabled in the BIOS. Check with your OS vendor to see if ISA auto configuration is supported.

Quick Boot in conjunction with the watchdog timer allows frozen systems or systems with temporary power loss to become operable again within a few seconds.



Note NumLock will always be off on boot up when Quick Boot is enabled.

Features and Settings That Can Affect Boot Time

The boot time of a system is dependent upon numerous system settings as well as devices attached to a system.. This section addresses some devices and settings that can increase or decrease a system's boot time.

Add-On Cards With BIOS Extensions

Some add-on cards have an integrated BIOS extension. The most common examples are SCSI controllers and network cards with boot ROMs. During POST, the BIOS executes the card's extension code. This extension code is third-party code, which is beyond RTD's control. The BIOS extension will most likely increase the boot time. Exactly how much it increases boot time will depend on the particular card and firmware version.

VGA Controller

VGA controllers have a VGA BIOS that must be initialized during POST. It can take some time to initialize the VGA BIOS. Exactly how long will depend on the particular VGA controller and BIOS version.

Hard Drive Type

During IDE initialization, each IDE device must be probed. Some devices take longer to probe. 2.5-inch hard drives tend to take longer than 3.5-inch ones, because they spin at a lower RPM.

Monitor Type

Some monitors take a while to power on. Desktop flat panels are especially slow. This does not affect the actual boot time of the CPU. However, the CPU may boot before the monitor powers on.

ESCD Updates

On the Geode BIOS, extended system configuration data (ESCD) is stored in the onboard flash. When the system configuration changes, this information must be updated. If an update is necessary, it will happen at the end of POST (the BIOS will display an "Updating ESCD..." message). The ESCD update takes a few seconds and increases the boot time. Once the ESCD is updated, boot times will return to normal.

ESCD updates only happen when the system configuration changes. They do not happen spuriously. They are usually triggered by adding or removing a PCI device from a stack. Updates can also be triggered by altering the Plug-n-Play configuration of the BIOS.

Boot Device Order

The BIOS contains a list of devices to try booting from. If you wish to boot to a particular device (for example, a hard drive), make sure that it is first in the boot order. This will speed up boot times.

Configuring with the RTD Enhanced Award BIOS

The cpuModule Setup program allows you to customize the cpuModule's configuration. Selections made in Setup are stored on the board and are read by the BIOS at power-on.

Starting Setup

You can run Setup by rebooting the cpuModule and pressing **Delete**. When you are finished with Setup, save your changes and exit. The system will automatically reboot.

Using the Setup Program

All displays in Setup consist of two areas. The left area lists the available selections. The right area displays help messages which you should always read.

Field Selection

You move between fields in Setup using the keys listed below.

Table 27 Setup Keys

Key	Function
→, ←, ↓, ↑	Move between fields
+, -, PgUp, PgDn	Selects next/previous values in fields
Enter	Go to the submenu for the field
Esc	To previous menu then to exit menu

Main Menu Setup Fields

The following is a list of Main Menu Setup fields.

Table 28 Main Menu Setup Fields

Field	Active Keys	Selections
Standard CMOS Setup	Press Enter to select	Access commonly used settings for the floppy drives, hard disks, and video.
BIOS Features Setup	Press Enter to select	Access settings for BIOS features such as boot sequence, keyboard options, and test options.
Chipset Features Setup	Press Enter to select	Set chipset specific options.
Power Management Setup	Press Enter to select	Set power management options.
PnP/PCI Configuration	Press Enter to select	Set PnP and PCI options.
Integrated Peripherals	Press Enter to select	Set I/O device options.
Supervisor Password	Press Enter to select	Set supervisor access password.
User Password	Press Enter to select	Set user access password.
IDE HDD Auto Detection	Press Enter to select	Have the BIOS detect the IDE hard disks connected to the system.
Save and Exit Setup	Press Enter to select	Save your changes and exit Setup.
Exit without Saving	Press Enter to select	Exit Setup without saving changes.



Note Future BIOS versions may have slightly different setup menus and options.

Standard CMOS Setup

Table 29 provides an alphabetical list of Standard CMOS Setup fields.

Table 29 Standard CMOS Setup Fields

Field	Active Keys	Selections	Default
Date	0...9, Enter	Sets the date with the format: <ul style="list-style-type: none"> month/day/year You must connect a backup battery or this setting will be lost at power down. 	—
Time	0...9, Enter	Sets the time with the format: <ul style="list-style-type: none"> hour: minute: second You must connect a backup battery or this setting will be lost at power down. 	—
Hard Disk Primary Master Primary Slave Secondary Master Secondary Slave	+, -, PgUp, PgDn	Selects the IDE hard disk type for each interface. An interface must have a master before a slave can be added. Ensure that you configure the drive jumpers correctly as master or slave and primary or secondary. Selections are: <ul style="list-style-type: none"> None Auto (Auto detect drive parameters; not all drives can be auto detected) 1–45 Standard drive types USER (User enters drive parameters) 	Auto
Drive A Drive B	+, -, PgUp, PgDn	Selects the format of each floppy disk. Selections are: <ul style="list-style-type: none"> None 360 KB, 5.25-inch Floppy 1.2 MB, 5.25-inch Floppy 720 KB, 3.5-inch Floppy 1.44/1.25 MB, 3.5-inch Floppy 2.88 MB, 3.5-inch Floppy 	1.44 MB, 3.5-inch
Video	+, -, PgUp, PgDn	Selects the Video format used during POST and the DOS prompt. <ul style="list-style-type: none"> EGA/VGA CGA 40 CGA 80 MONO 	EGA/ VGA
Halt On	+, -, PgUp, PgDn	Selects the type of errors which will halt the CPU during POST. User will need to press F1 for booting to continue. <ul style="list-style-type: none"> No Errors All, But Keyboard All, But Diskette All, But Disk/Key All Errors 	No Errors

BIOS Features Setup

Table 30 provides a list of BIOS Features Setup fields.

Table 30 BIOS Feature Setup Fields

Field	Active Keys	Selections	Default
Virus Warning	+ , - , PgUp, PgDn	Enable or disable virus warning: <ul style="list-style-type: none"> • Enable—Warn if boot sector or partition table is being modified • Disable—Allow boot sector or partition table modification 	Disabled
CPU Internal Cache	+ , - , PgUp, PgDn	Enable or disable CPU internal cache: <ul style="list-style-type: none"> • Enable—Enable CPU internal 16 KB cache • Disable—Disable CPU internal 16 KB cache 	Enabled
Cyrix 6x86/MII CPUID	+ , - , PgUp, PgDn	Enable or disable the CPUID instruction: <ul style="list-style-type: none"> • Enable—CPU will report itself as a Cyrix processor when the CPUID instruction is executed. Enabling the Cyrix CPUID allows older operating systems that might not recognize the Geode processor to run without an issue. • Disable—CPU will report itself as a Geode processor. 	Enabled
Boot Sequence	+ , - , PgUp, PgDn	Select from the options the boot sequence for the CPU.	A, C, SCSI
Swap Floppy Drive	+ , - , PgUp, PgDn	Swap floppy drive A: and B: <ul style="list-style-type: none"> • Enable—Floppy connected after the twist in the floppy wire will be Drive B: and floppy connected before the twist in the floppy wire will be Drive A: • Disable (Normal)—Floppy connected after the twist in the floppy wire will be Drive A: and floppy connected after the twist in the floppy wire will be Drive B: Note: This only works with two floppies installed.	Disabled
Boot Up Numlock Status	+ , - , PgUp, PgDn	Set keypad numlock status after boot: <ul style="list-style-type: none"> • On—Keypad is number keys • Off—Keypad is cursors keys 	Off
Gate A20 Option	+ , - , PgUp, PgDn	Select gate A20 options: <ul style="list-style-type: none"> • Normal—Use keyboard controller to control A20 gate • Fast—Allow chipset to control A20 gate 	Fast
Security Option	+ , - , PgUp, PgDn	Limit access with password to system and setup, or just setup: <ul style="list-style-type: none"> • System—The system will not boot and access to setup will be denied if the correct password is not entered at the prompt • Setup—The system will boot but, access to setup will be denied if the correct password is not entered at the prompt Note: To disable security, select Password setting at the main menu and then you will be asked to enter a password. Do not type anything, just press Enter and it will disable security. Once security is disabled, you can boot and enter setup freely.	Setup
Report No FDD for Win95	+ , - , PgUp, PgDn	Enable reporting that there is no floppy disk drives to Win95: <ul style="list-style-type: none"> • Yes—Report to Win 95 if there are no floppies • No—Do not report to Win 95 if there are no floppies 	Yes

Table 30 BIOS Feature Setup Fields (cont'd)

Field	Active Keys	Selections	Default
Full Screen Logo Show	+, -, PgUp, PgDn	Enable or disable the full screen RTD logo. <ul style="list-style-type: none"> • Enable • Disable 	Disabled
Quick Boot	+, -, PgUp, PgDn	Enable or Disable Quick Boot: <ul style="list-style-type: none"> • Disable • Enable Note: Enabling Quick Boot overrides Extended Memory Test Selection and disables Boot Up Numlock Status.	Disabled
Extended Memory Test	+, -, PgUp, PgDn	Enable or Disable Extended Memory Test: <ul style="list-style-type: none"> • Disable • Enable 	Disabled
ISA Plug-n-Play Support	+, -, PgUp, PgDn	Enable or Disable ISA Plug-n-Play Support: <ul style="list-style-type: none"> • Disable • Enable 	Enabled
BIOS Shadowing	+, -, PgUp, PgDn	Enable or disable copying slow ROMs to fast DRAM for the following memory areas: <ul style="list-style-type: none"> • Video BIOS • C8000–CBFFFh • CC000–CFFFFh • D0000–D3FFFh • D4000–D7FFFh • D8000–DBFFFh • DC000–DFFFFh 	Enabled Disabled Disabled Disabled Disabled Disabled Disabled
Cyrix 6x86/MII CPUID	+, -, PgUp, PgDn	Enable or disable the CPUID instruction: <ul style="list-style-type: none"> • Enable—CPU will report itself as a Cyrix processor when the CPUID instruction is executed. Enabling the Cyrix CPUID allows older operating systems that might not recognize the Geode processor to run without an issue. • Disable—CPU will report itself as a Geode processor. 	Enabled

Chipset Features Setup

Table 31 provides a list of Chipset Features Setup fields.

Table 31 Chipset Features Setup Fields¹

Field	Active Keys	Selections	Default
16-bit I/O Recovery (Clocks)	+, -, PgUp, PgDn	Set the recovery time for 16-bit I/O cycles. Selection is from 1 to 16 clocks.	5
8-bit I/O Recovery (Clocks)	+, -, PgUp, PgDn	Set the recovery time for 8-bit I/O cycles. Selection is from 1 to 16 clocks.	5

1. Recovery time is the length of time, measured in CPU clocks, that the system will delay after the completion of an input/output request. This delay takes place because the CPU is operating so much faster than the I/O bus that the CPU must be delayed to allow for the completion of the I/O.

Power Management Setup Fields

Table 32 provides a list of Power Management Setup fields.

Table 32 Power Management Setup Fields

Field	Active Keys	Selections	Default
Power Management	+ , - , PgUp, PgDn	Select power management mode: <ul style="list-style-type: none"> • Disable—power management off • Min Saving—minimum power savings, maximum performance • Max Saving—maximum power savings, minimum performance • User Defined—user selects the power management functions to suit the application 	Disabled
Doze Mode	+ , - , PgUp, PgDn	Select inactivity time delay before entering doze mode: <ul style="list-style-type: none"> • Disable—doze mode off • 1—1 second • 2—2 seconds • 4—4 seconds • 8—8 seconds • 10—10 seconds • 12—12 seconds • 15—15 seconds • 16—16 seconds 	Disabled
Standby Mode	+ , - , PgUp, PgDn	Select inactivity time delay before entering standby mode: <ul style="list-style-type: none"> • Disable—Standby mode off • 1—1 minute • 2—2 minutes • 4—4 minutes • 8—8 minutes • 10—10 minutes • 12—12 minutes • 15—15 minutes • 16—16 minutes • 20—20 minutes • 30—30 minutes • 40—40 minutes • 60—60 minutes 	Disabled
HDD Power Down	+ , - , PgUp, PgDn	Select inactivity time delay before hard disk power down: <ul style="list-style-type: none"> • Disable—HDD power down off • 1—1 minute • 2—2 minutes • 4—4 minutes • 8—8 minutes • 10—10 minutes • 12—12 minutes • 15—15 minutes • 16—16 minutes • 20—20 minutes • 30—30 minutes • 40—40 minutes • 60—60 minutes 	Disabled

Table 32 Power Management Setup Fields (cont'd)

Field	Active Keys	Selections	Default
Modem use IRQ	+, -, PgUp, PgDn	Select IRQ for modem wakeup: <ul style="list-style-type: none"> • NA—not available • 3—IRQ 3 • 4—IRQ 4 • 5—IRQ 5 • 7—IRQ 7 • 9—IRQ 9 • 10—IRQ 10 • 11—IRQ 11 	N/A
Throttle Duty Cycle	+, -, PgUp, PgDn	Select throttle duty cycle: <ul style="list-style-type: none"> • 12.5—12.5% minimum savings • 33.3—33.3% • 50.0—50.0% • 75.0—75.0% maximum savings 	33.3%
IRQ that will bring the CPU out of power management	+, -, PgUp, PgDn	Select IRQs that will wake the CPU out of suspend mode: <ul style="list-style-type: none"> • IRQ 1 • IRQ 3 • IRQ 4 • IRQ 5 • IRQ 6 • IRQ 7 • IRQ 9 • IRQ 10 • IRQ 11 • IRQ 12 • IRQ 13 • IRQ 14 • IRQ 15 	On Off Off Off Off Off Off Off Off Off Off Off Off

PnP/PCI Configuration Setup Fields

Table 33 provides a list of PnP/PCI Configuration Setup fields.

Table 33 PnP/PCI Configuration Setup Fields

Field	Active Keys	Selections	Default
PnP OS Installed	+ , - , PgUp, PgDn	Select if you are using a PnP aware operating system. If you select Yes the Operating System will change the I/O assignments made in the BIOS. <ul style="list-style-type: none"> • Yes—Using a PnP operating system such as Microsoft Windows 95/98 • No—Not using a PnP operating system 	No
Resources Controlled By	+ , - , PgUp, PgDn	How IRQ and DMA resources are allocated <ul style="list-style-type: none"> • Auto—BIOS configures resources • Manual—User configures resources 	Auto
Reset Configuration Data	+ , - , PgUp, PgDn	Select Enable to clear the Extended System Configuration Data (ESCD) area. This will make the CPU search for legacy devices and store the updated info. This field will automatically return to disable after the next boot.	Disabled
PCI IRQ Activated By	+ , - , PgUp, PgDn	Select if PCI interrupts are level or edge sensitive.	Level

Integrated Peripherals Setup Fields

Table 34 provides a list of Integrated Peripherals Setup fields.

Table 34 Integrated Peripherals Setup Fields

Field	Active Keys	Selections	Default
IDE HDD Block Mode	+ , -, PgUp, PgDn	Allow the IDE controller to use fast block mode to transfer data to and from the hard disk. <ul style="list-style-type: none"> • Enable—IDE controller uses block mode • Disable—IDE controller does not uses block mode 	Enabled
Onboard Primary IDE	+ , -, PgUp, PgDn	Enable or disable the onboard primary IDE controller. <ul style="list-style-type: none"> • Enable • Disable 	Enabled
Primary Master/Slave Drive PIO Mode	+ , -, PgUp, PgDn	Control the PIO mode used to access the hard drive. <ul style="list-style-type: none"> • Auto • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4 	Auto
IDE Primary Master/Slave UDMA	+ , -, PgUp, PgDn	Enable or disable UltraDMA transfer modes for attached IDE devices. <ul style="list-style-type: none"> • Auto • Disable 	Auto
Onboard Secondary IDE	+ , -, PgUp, PgDn	Enable or disable the ATA/IDE Disk Chip socket. <ul style="list-style-type: none"> • Enable • Disable 	Enabled
ATA/IDE Disk Chip Mode	+ , -, PgUp, PgDn	Select the mode of the ATA/IDE Disk Chip socket. <ul style="list-style-type: none"> • Multi-word DMA mode • PIO mode 	MW-DMA
Write Protect Feature (PIO Mode Only)	+ , -, PgUp, PgDn	Enable or disable write protection for PIO mode Disk Chips <ul style="list-style-type: none"> • Enable • Disable 	Disabled
Keyboard Input Clock	+ , -, PgUp, PgDn	Select the clock to be used for the keyboard controller. <ul style="list-style-type: none"> • 8—8 MHz (default) • 12—12 MHz • 16—16 MHz 	8 MHz
Onboard Serial Port 1	+ , -, PgUp, PgDn	Serial Port 1 connector (CN7) settings. <ul style="list-style-type: none"> • Disable—Serial port not used • Auto—BIOS/OS controls operation • 3F8/IRQ 4—Address 3F8h and interrupt 4 • 2F8/IRQ 3—Address 2F8h and interrupt 3 • 3E8/IRQ 4—Address 3E8h and interrupt 4 • 2E8/IRQ 3—Address 2E8h and interrupt 3 	3F8h/ IRQ4
Onboard Serial Port 1 Mode	+ , -, PgUp, PgDn	Select mode for onboard serial port 1. <ul style="list-style-type: none"> • RS-232—RS-232 driver/receiver enabled • RS-422/485—RS-422/485 driver/receiver enabled 	RS-232

Table 34 Integrated Peripherals Setup Fields (cont'd)

Field	Active Keys	Selections	Default
Onboard Serial Port 2	+ , - , PgUp, PgDn	Serial Port 2 connector (CN8) settings. <ul style="list-style-type: none"> • Disable—serial port not used • Auto—BIOS/OS controls operation • 3F8/IRQ 4—address 3F8h and interrupt 4 • 2F8/IRQ 3—address 2F8h and interrupt 3 • 3E8/IRQ 4—address 3E8h and interrupt 4 • 2E8/IRQ 3—address 2E8h and interrupt 3 	2F8h/ IRQ3
Onboard Serial Port 2 Mode	+ , - , PgUp, PgDn	Select mode for onboard serial port 2. <ul style="list-style-type: none"> • RS-232—RS-232 driver/receiver enabled • RS-422/485—RS-422/485 driver/receiver enabled 	RS-232
multiPort (CN6)	+ , - , PgUp, PgDn	Select the function of the multiPort. <ul style="list-style-type: none"> • Parallel • Floppy • aDIO • Disabled 	Parallel
Parallel Port (Parallel mode only)	+ , - , PgUp, PgDn	Parallel port settings. <ul style="list-style-type: none"> • 378/IRQ7—address 378h and interrupt 7 • 278/IRQ5—address 278h and interrupt 5 • 3BC/IRQ7—address 3BCh and interrupt 7 • Disabled 	378/ IRQ7
Parallel Port Mode (Parallel mode only)	+ , - , PgUp, PgDn	Select parallel port mode. <ul style="list-style-type: none"> • ECP + EPP • SPP • EPP 1.7 • EPP 1.9 • ECP 	ECP + EPP
ECP Mode Use DMA (Parallel mode with ECP only)	+ , - , PgUp, PgDn	Select the DMA channel used in ECP mode. <ul style="list-style-type: none"> • 3 • 1 	3
IRQ (aDIO mode only)	+ , - , PgUp, PgDn	Select the IRQ line used by the aDIO interface. <ul style="list-style-type: none"> • Disabled • IRQ5 • IRQ7 • IRQ10 • IRQ11 • IRQ12 	Disabled
Fail Safe Boot ROM	+ , - , PgUp, PgDn	Enable or disable the Fail Safe Boot ROM. <ul style="list-style-type: none"> • Disabled • Enabled 	Disabled
Video Init. Priority	+ , - , PgUp, PgDn	Select primary video controller. <ul style="list-style-type: none"> • Onboard • External 	Onboard
Video Memory Size	+ , - , PgUp, PgDn	Select video memory size. <ul style="list-style-type: none"> • 1.5 M • 2.5 M • 4.0 M 	4.0 M

Table 34 Integrated Peripherals Setup Fields (cont'd)

Field	Active Keys	Selections	Default
Flat Panel Resolution	+, -, PgUp, PgDn	Select flat panel resolution. <ul style="list-style-type: none">• 640 x 480• 800 x 600• 1024 x 768• Disabled	640 x 480

Supported Video Resolutions and BIOS Settings

Table 35 provides a list of supported video resolutions and minimum BIOS settings.

Table 35 Supported Video Resolutions and BIOS Settings

Resolution	Colors	Refresh Rate	Allocated Video Memory (BIOS Setting)
640 x 480	256	60	1.5 MB
640 x 480	256	72	1.5 MB
640 x 480	256	75	1.5 MB
640 x 480	256	85	1.5 MB
640 x 480	64 K	60	1.5 MB
640 x 480	64 K	72	1.5 MB
640 x 480	64 K	75	1.5 MB
640 x 480	64 K	85	1.5 MB
800 x 600	256	60	1.5 MB
800 x 600	256	72	1.5 MB
800 x 600	256	75	1.5 MB
800 x 600	256	85	1.5 MB
800 x 600	64 K	60	1.5 MB
800 x 600	64 K	72	1.5 MB
800 x 600	64 K	75	1.5 MB
800 x 600	64 K	85	1.5 MB
1024 x 768	256	60	1.5 MB
1024 x 768	256	70	1.5 MB
1024 x 768	256	75	1.5 MB
1024 x 768	256	85	1.5 MB
1024 x 768	64 K	60	2.5 MB
1024 x 768	64 K	70	2.5 MB
1024 x 768	64 K	75	2.5 MB
1024 x 768	64 K	85	2.5 MB
1280 x 1024	256	60	4.0 MB
1280 x 1024	256	70	4.0 MB
1280 x 1024	256	75	4.0 MB
1280 x 1024	256	85	4.0 MB
1280 x 1024	64 K	60	4.0 MB
1280 x 1024	64 K	75	4.0 MB
1280 x 1024	64 K	85	4.0 MB



Note If flat panel video is enabled, the resolution may be limited by the flat panel type.

Chapter 5 Using the cpuModule

This chapter provides information for users who wish to develop their own applications programs for the CMC26686CX cpuModule.

This chapter includes information on the following topics:

- Memory map
- I/O address map
- Interrupts
- Power on self tests (POSTs)
- System functions (watchdog timer, real time clock)
- Configuring the ATA/IDE Disk Chip socket
- Utility programs

Memory Map

The ISA portion of the cpuModule addresses memory using 24 address lines. This allows a maximum of 2^{24} locations, or 16 MB of memory.

Table 36 shows how memory in the first megabyte is allocated in the system.

Table 36 First Megabyte Memory Map

Address (hex)	Description
C0000–FFFFh ROM	256 KB BIOS in Flash EPROM, shadowed into DRAM during runtime.
C0000–EFFFFh	Run time user memory space. Usually, memory between C0000h and C7FFFh is used for the BIOS of add-on VGA video cards.
A0000–BFFFFh	Normally used for video RAM as follows: EGA/VGA 0A0000–0AFFFFh Monochrome 0B0000–0B7FFFh CGA 0B8000–0BFFFFh
00502–9FFFFh	DOS reserved memory area
00400–00501h	BIOS data area
00000–003FFh	Interrupt vector area

Memory beyond the first megabyte can be accessed in real mode by using EMS or a similar memory manager. See your OS or programming language references for information on memory managers.

I/O Address Map

As with all standard PC/104 boards, the I/O space is addressed by 10 address lines (SA0–SA9). This allows 2¹⁰ or 1024 distinct I/O addresses. Any add-on modules you install must therefore use I/O addresses in the range of 0–1023 (decimal) or 000–3FF (hex).



Note If you add any PC/104 modules or other peripherals to the system you must ensure they do not use reserved addresses listed below, or malfunctions will occur. The exception to this is if the resource has been released by the user.

Table 37 lists I/O addresses reserved for the CMC26686CX cpuModule.

Table 37 I/O Addresses Reserved for the CMC26686CX cpuModule

Address Range (hex)	Bytes	Device
000–00Fh	16	DMA Controller
010–01Fh	16	Reserved for CPU
020–021h	2	Interrupt Controller 1
022–02Fh	13	Reserved
040–043h	4	Timer
060–064h	5	Keyboard Interface
070–071h	2	Real Time Clock Port
080–08Fh	16	DMA Page Register
0A0–0A1h	2	Interrupt Controller 2
0C0–0DFh	32	DMA Controller 2
0F0–0FFh	16	Math Coprocessor
100–101h	2	Video Initialization
1F0–1FFh	16	Hard Disk ¹
200–201h	2	Reserved
238–23Bh	4	Bus Mouse ²
2E8–2EFh	8	Serial Port ³
2F8–2FFh	8	Serial Port ³
3E8–3EFh	8	Serial Port ³
3F0–3F7h	8	Floppy Disk ¹
3F8–3FFh	8	Serial Port ³

1. If a floppy or IDE controller is not connected to the system, the I/O addresses listed will not be occupied.
2. If a PS/2 mouse is not connected to the system, the I/O addresses listed will not be occupied.
3. Only one of the I/O addresses shown for a serial port is active at any time. You can use Setup to select which one is active or to disable it entirely.

Hardware Interrupts



Note If you add any PC/104 modules or other peripherals to the system, you must ensure they do not use interrupts needed by the cpuModule, or malfunctions will occur.

The CMC26686CX cpuModule supports the standard PC interrupts listed in Table 38. Interrupts not in use by hardware on the cpuModule itself are listed as available.

Table 38 Hardware Interrupts Used on the CMC26686CX cpuModule

Interrupt	Normal Use	Source
0	Timer 0	Onboard ISA device
1	Keyboard	Onboard ISA device
2	Cascade of IRQ 8–15	Onboard ISA device
3	COM2	Onboard ISA device
4	COM1	Onboard ISA device
5	Available	XT bus
6	Floppy ¹	XT bus
7	Printer	Onboard ISA device
8	Real Time Clock	Onboard ISA device
9	Available, routed to IRQ 2	XT bus
10	Available	AT bus
11	Available	AT bus
12	Bus Mouse	Onboard ISA device
14	Primary IDE hard disk ²	AT bus
15	Available sometimes used as secondary IDE hard disk	AT bus

1. Floppy disk interrupt, INT6, is available for use if no floppy disk is present in the system and floppy disk is disabled in Setup.
2. Hard disk interrupt, INT14, is available for use if no hard disk drive is present in the system and hard disk is disabled in Setup.



Note The cpuModule has onboard PCI devices that will claim IRQ lines. In some instances, a PCI device will claim an IRQ line that is required by a legacy device. To reserve an IRQ for a legacy device, refer to the PnP/PCI Configuration Setup fields in the BIOS (page 56).

The RTD Enhanced Award BIOS

The RTD Enhanced Award BIOS is software that interfaces hardware-specific features of the cpuModule to an operating system (OS). Physically, the BIOS software is stored in a Flash EPROM on the cpuModule. Functions of the BIOS are divided into two parts.

The first part of the BIOS is known as POST (power-on self-test) software, and it is active from the time power is applied until an OS boots (begins execution). POST software performs a series of hardware tests, sets up the machine as defined in Setup, and begins the boot of the OS.

The second part of the BIOS is known as the CORE BIOS. It is the normal interface between cpuModule hardware and the OS which is in control. It is active from the time the OS boots until the cpuModule is turned off. The CORE BIOS provides the system with a series of software interrupts to control various hardware devices.

The following sections discuss the sections of the BIOS in more detail and describe features of the BIOS that may be useful to you in developing applications.

Power On Self Tests (POSTs)

POST Codes

Each POST Code represents a series of events that take place in a system during the POST. If the POST fails during a particular POST Code, the system will not boot as expected.

The BIOS uses I/O port 80h to store the active POST Code. A POST Code board is a tool that is used to display the POST Codes on I/O port 80h. This is usually accomplished with two 7-segment LEDs. Such a board is useful for debugging a system that is unable to boot.

POST Messages

During the POST, if the BIOS detects an error that you must fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP



Note *If the BIOS is set to Halt On no errors, this message will not be displayed. Halt On no errors is set by default in the BIOS.*

POST Beep Codes

Currently there are two kinds of beep codes in the BIOS.

- **Single long beep followed by three short beeps.** This beep code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information.
- **Single long beep repeatedly.** This code indicates that a DRAM error has occurred.

Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS or Flash has become corrupt.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press **Enter**. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Reboot the system.

DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

BIOS ROM CHECKSUM ERROR - SYSTEM HALTED

The checksum of ROM address F0000–FFFFFh is bad.

MEMORY TEST FAIL

BIOS reports the memory test fail if the onboard memory is tested error.

Common POST Codes

Table 39 is a list of common POST Codes. Some POST Codes that are not listed in the table. POST Codes may change between BIOS versions.

Table 39 RTD Enhanced Award BIOS POST Codes

POST (hex)	Description
C0h	<ol style="list-style-type: none"> 1. Turn off OEM specific cache and shadow memory. 2. Initialize all the standard devices with default values. Standard devices include: <ul style="list-style-type: none"> • DMA controller (8237) • Programmable interrupt controller (8259) • Programmable interval timer (8254) • Real time clock chip
C1h	Auto-detection of onboard DRAM and cache
C3h	<ol style="list-style-type: none"> 1. Test system BIOS checksum. 2. Test the first 256 KB DRAM. 3. Expand the compressed codes into temporary DRAM area including the compressed System BIOS and option ROMs.
C5h	Copy the BIOS from ROM into E0000–FFFFh shadow RAM so that POST will go faster
01h	Clear base memory 0~640 KB
05h	<ol style="list-style-type: none"> 1. Keyboard controller self-test. 2. Enable keyboard interface.
07h	Verifies CMOSes basic read/write functionality
09h	Program the configuration registers of Cyrix CPU.
0Ah	<ol style="list-style-type: none"> 1. Initialize the first 32 interrupt vectors with corresponding interrupt handlers. 2. Issue CPUID instruction to identify CPU type. 3. Early power management initialization (OEM specific).
0Bh	<ol style="list-style-type: none"> 1. Verify the real time clock time is valid or not. 2. Detect bad battery. 3. Read CMOS data into BIOS stack area. 4. PnP initialization including (PnP BIOS only): <ul style="list-style-type: none"> –Assign CSN to PnP ISA card –Create resource map from ESCD 5. Assign I/O and memory for PCI devices .
0Ch	Initialization of the BIOS Data Area (40:00–40:FFh)
0Dh	<ol style="list-style-type: none"> 1. Program some of the chipset's value according to Setup (early setup value program). 2. Measure CPU speed for display and decide the system clock speed. 3. Video initialization including Monochrome, CGA, EGA/VGA. If no display device found, the speaker will beep, which consists of one single long beep followed by two short beeps.
0Eh	<ol style="list-style-type: none"> 1. Test video RAM (if monochrome display device found). 2. Show messages including: <ul style="list-style-type: none"> –Award Logo –copyright string –BIOS Date code –P/N –RTD sign on messages –CPU brand, type, and speed
0Fh	DMA channel 0 test
10h	DMA channel 1 test
11h	DMA page registers test

Table 39 RTD Enhanced Award BIOS POST Codes (cont'd)

POST (hex)	Description
14h	Test 8254 Timer 0 Counter 2
15h	Test 8259 interrupt mask bits for channel 1
16h	Test 8259 interrupt mask bits for channel 2
19h	Test 8259 functionality
30h	Detect base memory and extended memory size
31h	<ol style="list-style-type: none"> 1. Test base memory from 256 KB to 640 KB. 2. Test extended memory from 1 MB to the top of memory.
32h	<ol style="list-style-type: none"> 1. Display the Award Plug-n-Play BIOS Extension message. 2. Program onboard super I/O chip, including COM ports, LPT ports, and FDD port according to setup value.
41h	Initialize floppy disk drive controller
42h	Initialize hard drive controller
43h	Initialize serial and parallel ports
45h	Initialize math coprocessor
50h	Write all CMOS values currently in the BIOS stack area back into the CMOS
52h	<ol style="list-style-type: none"> 1. Initialize all ISA ROMs. 2. Later PCI initialization: <ul style="list-style-type: none"> –Assign IRQ to PCI devices –Initialize all PCI ROMs 3. PnP initialization: <ul style="list-style-type: none"> –Assign I/O, memory, IRQ, and DMA to PnP ISA devices –Initialize all PnP ISA ROMs 4. Program shadows RAM according to Setup settings. 5. Program parity according to Setup setting. 6. Power Management Initialization: <ul style="list-style-type: none"> –Enable/Disable global PM –APM interface initialization
53h	Initialize time value in BIOS data area by translating the real time clock time value into a timer tick value
55h	Load BIOS extensions
60h	Setup virus protection (boot sector protection) functionality according to Setup setting
3Ch	Set flag to allow users to enter CMOS Setup Utility
3Dh	<ol style="list-style-type: none"> 1. Initialize keyboard. 2. Install PS/2 mouse.
41h	Enable FDD and detect media type
4Eh	If there is any error detected (such as video, kb...), show all the error messages on the screen and wait for user to press F1 key
4Fh	If password is needed, ask for password.
BEh	Program defaults values into chipset.
BFh	Program the rest of the chipset's value according to Setup (later setup value program).
FFh	System Booting INT 19

Direct Hardware Control

Some of the cpuModule hardware is controlled directly without using BIOS routines. These include Advanced Digital I/O (aDIO™), watchdog timer, real time clock control, and parallel port control.

Advanced Digital I/O Ports (aDIO™)

Ensure that the BIOS setup has the multiPort set to aDIO mode. This board supports 16 bits of TTL/CMOS compatible digital I/O (TTL signaling). Use the BIOS setup to set the multiPort into its aDIO mode. These I/O lines are grouped into two ports, Port 0 and Port 1. Port 0 is bit programmable; Port 1 is byte programmable. Port 0 supports RTD's Advanced Digital Interrupt modes. The two modes are match and event. Match mode generates an interrupt when an 8-bit pattern is received in parallel that matches the match mask register. Event mode generates an interrupt when a change occurs on any bit. In either mode, masking can be used to monitor selected lines.

When the CPU boots, all digital I/O lines are programmed as inputs, meaning that the digital I/O line's initial state is undetermined. If the digital I/O lines must power up to a known state, an external 10 kΩ resistor must be added to pull the line high or low.

The 8-bit control read/write registers for the digital I/O lines are located from I/O address 450h to 453h. These registers are written to zero upon power up. From 450h to 453h, the name of these registers are **Port 0 data**, **Port 1 data**, **Multi-Function**, and **DIO-Control** register.



Note RTD provides drivers that support the aDIO interface on popular operating systems. RTD recommends using these drivers instead of accessing the registers directly.

Digital I/O Register Set

Table 40 Port 0 Data I/O Address 450h

D7	D6	D5	D4	D3	D2	D1	D0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Port 0 Data register is a read/write bit direction programmable register. A particular bit can be set to input or output. A read of an input bit returns the value of port 0. A read of an output bit returns the last value written to Port 0. A write to an output bit sends that value to port 0.

Table 41 Port 1 Data I/O Address 451h

D7	D6	D5	D4	D3	D2	D1	D0
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Port 1 Data register is a read/write byte direction programmable register. A read on this register when it is programmed to input will read the value at the multiPort connector. A write on this register when it is programmed as output will write the value to the multiPort connector. A read on this register when it is set to output will read the last value sent to the multiPort connector.

Table 42 Multi-Function I/O Address 452h

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

The multi-function register is a read/write register whose contents are set by the DIO-Control register. See the DIO-Control register description for a description of this register.

Table 43 DIO-Control I/O Address 453h—Read Access

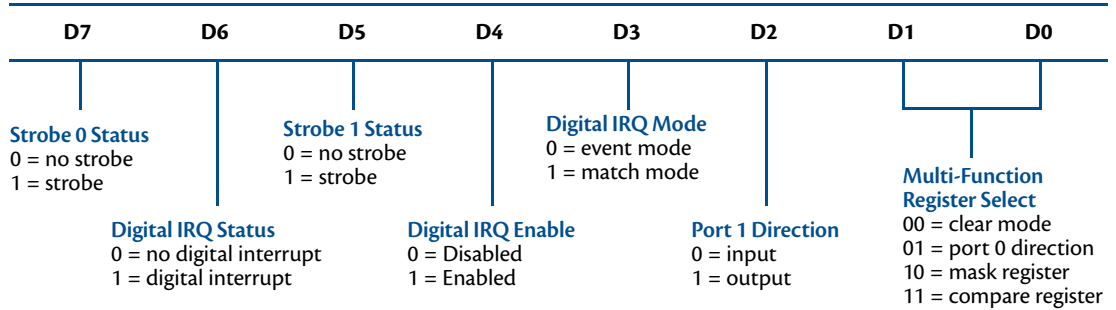


Table 44 DIO-Control I/O Address 453h—Write Access

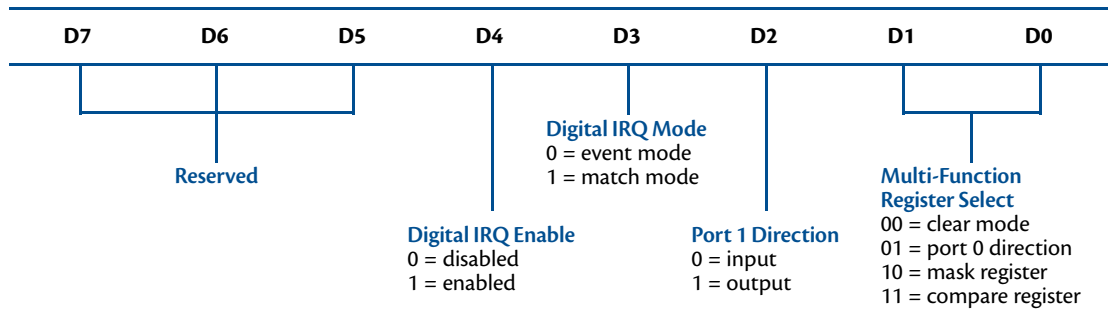


Table 45 Multi-Function at Address 452h¹

read/write	00 clear	X	X	X	X	X	X	X	X
0 in, 1 out	01 Port 0 direction	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
0 no mask, 1 mask	10 DIO mask	M7	M6	M5	M4	M3	M2	M1	M0
read/write	11 compare	C7	C6	C5	C4	C3	C2	C1	C0

1. Contents based on bits D0 and D1 of DIO-Control.

Clear Register:

A read to this register Clears the IRQs and a write to this register sets the DIO-Compare, DIO- Mask, DIO-Control, Port 1, and Port 0 to zeros. A write to this register is used to clear the board.

Port 0 Direction Register:

Writing a zero to a bit in this register makes the corresponding pin of the multiPort connector an input. Writing a one to a bit in this register makes the corresponding pin of the multiPort connector an output.

Mask Register:

Writing a zero to a bit in this register will not mask off the corresponding bit in the DIO-Compare register. Writing a one to a bit in this register masks off the corresponding bit in the DIO-Compare register. When all bits are masked off the aDIOs comparator is disabled. This condition means Event and Match mode will not generate an interrupt. This register is used by Event and Match modes.

Compare Register:

A Read/Write register used for Match Mode. Bit values in this register that are not masked off are compared against the value on Port 0. A Match or Event causes bit 6 of DIO-Control to be set and if the aDIO is in Advanced interrupt mode, the Match or Event causes an interrupt.

Interrupts

The Digital I/O can use interrupts 5, 7, 10, 11, and 12. To use one of the 5 listed interrupts, set the interrupt(s) aside for an ISA legacy device. To set the interrupts aside, enter the BIOS under **PNP/PCI CONFIGURATION**. Select **Resources Controlled By** and change the interrupt(s) you wish to use to legacy ISA.

Advanced Digital Interrupts

There are three Advanced Digital Interrupt modes available. These three modes are Event, Match, and Strobe. The use of these three modes is to monitor state changes at the multiPort connector. One way to enable interrupts is to set bit 4 of the DIO-Control register to a 1 and select Event or Match mode. The other way to enable interrupts is explained in *Strobe Mode*.

Event Mode

When this mode is enabled, Port 0 is latched into the DIO-Compare register at 8.33 MHz. The aDIO circuitry includes deglitching logic. The deglitching requires pulses on Port 0 to be at least 120 ns in width. As long as changes are present longer than that, the event is guaranteed to register. Pulses as small as 60 ns can register as an event, but they must occur between the rising and falling edge of the 8.33 MHz clock. To enter Event mode, set bit 3 of the DIO-Control register to a zero.

Match Mode

When this mode is enabled, Port 0 is latched into the DIO-Compare register at 8.33 MHz. The aDIO circuitry includes deglitching logic. The deglitching requires pulses on Port 0 to be at least 120 ns in width. As long as changes are present longer than that, the match is guaranteed to register. Pulses as small as 60 ns can register as a match, but they must occur between the rising and falling edge of the 8.33 MHz clock. To enter Match mode, set bit 3 of the DIO-Control register to a one.



Note Make sure bit 3 is set BEFORE writing the DIO-Compare register. If you do not set bit 3 first, the contents of the DIO-Compare register could be lost because the Event mode latches in Port 0 into the DIO-Compare register at an 8.33 MHz rate.

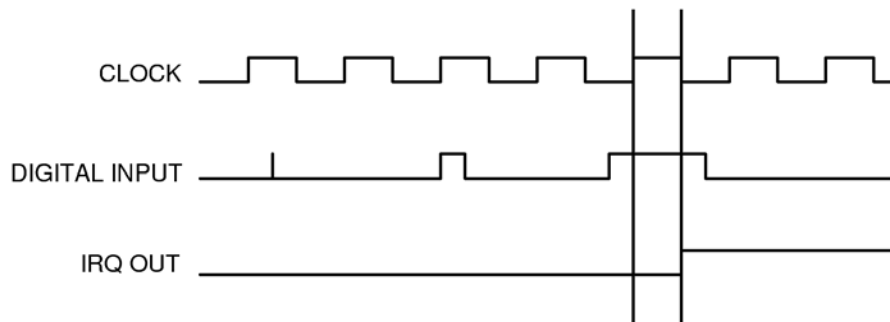


Figure 5 aDIO Match Mode

Strobe Mode

Another interrupt mode supported by aDIO is Strobe mode. You can enable Strobe mode by writing a **zero** to the Digital IRQ Enable bit of the DIO-Control register and a **one** to the Digital IRQ Mode bit in the DIO-Control register. What these writes do is to allow the strobe pin of the DIO connector to trigger an interrupt. A low to high transition on the strobe pin will cause an interrupt request. The request will remain high until the Clear Register is read from. Additionally, the Compare Register latched in the value at Port 0 when the Strobe pin made a low to high transition. No further strobes will be available until a read of the Compare Register is made. You must read the Compare Register, and then clear interrupts so that the latched value in the compare register is not lost.

Table 46 Interrupt Generation

Digital IRQ Mode	Digital IRQ Enable	Function
0	0	DIO Only
0	1	Event Mode
1	0	Strobe Mode
1	1	Match Mode

Basic Interrupt Information for Programmers

An interrupt is a subroutine called asynchronously by external hardware (usually an I/O device) during the execution of another application. The CPU halts execution of its current process by saving the system state and next instruction, and then jumps to the interrupt service routine, executes it, loads the saved system state and saved next instruction, and continues execution. Interrupts are good for handling infrequent events such as keyboard activity. Interrupts on this `cpuModule` are controlled by two Intel 8259-equivalent interrupt controllers containing 13 available interrupt request lines.

What happens when an interrupt occurs?

An `IRQx` pin on the PC/104 bus makes a low to high transition while the corresponding interrupt mask bit is unmasked and the PIC determines that the `IRQ` has priority, that is, the PIC interrupts the processor. The current code segment (`CS`), instruction pointer (`IP`), and flags are pushed onto the stack. The CPU then reads the 8-bit vector number from the PIC, and a new `CS` and `IP` are loaded from a vector—indicated by the vector number—from the interrupt vector table that exists in the lowest 1024 bytes of memory. The processor then begins executing instructions located at `CS:IP`. When the interrupt service routine is completed the `CS`, `IP`, and flags that were pushed onto the stack are popped from the stack into their appropriate registers and execution resumes from the point where it was interrupted.

How long does it take to respond to an interrupt?

A DOS system can respond to an interrupt between 6 and 15 μ s. A Windows system can take a much longer time when a service routine has been installed by a device driver implemented as a DLL—from 250 to 1500 μ s or longer. The time the CPU spends in the interrupt depends on the efficiency of the code in the ISR. These numbers are general guidelines and will fluctuate depending on operating system and version. Minimum time between two `IRQ` requests is 125 ns per ISA specification.

Interrupt Request Lines

To allow different peripheral devices to generate interrupts on the same computer, the ISA bus has eight different interrupt request (`IRQ`) lines. On the ISA bus, a transition from low to high on one of these lines generates an interrupt request, which is handled by the PC's interrupt controller. On the PCI bus, an interrupt request is level-triggered.

The interrupt controller checks to see if interrupts are to be acknowledged from that `IRQ` and, if another interrupt is already in progress, it decides if the new request should supersede the one in progress or if it has to wait until the one in progress is done. This prioritizing allows an interrupt to be interrupted if the second request has a higher priority. The priority level is based on the number of the `IRQ`; `IRQ0` has the highest priority, `IRQ1` is second-highest, and so on through `IRQ7`, which has the lowest. Many of the `IRQs` are used by the standard system resources. `IRQ0` is used by the system timer, `IRQ1` is used by the keyboard, `IRQ3` by `COM2`, `IRQ4` by `COM1`, and `IRQ6` by the disk drives. Therefore, it is important to know which `IRQ` lines are available in your system for use by the `cpuModule`.

Intel 8259 Programmable Interrupt Controller

The chip responsible for handling interrupt requests in the PC is the Intel 8259 Programmable Interrupt Controller. To use interrupts, you need to know how to read and set the Intel 8259's interrupt mask register (`IMR`) and how to send the end-of-interrupt (`EOI`) command to the Intel 8259.

Each bit in the `IMR` contains the mask status of an `IRQ` line; bit 0 is for `IRQ0`, bit 1 is for `IRQ1`, and so on. If a bit is set (1), then the corresponding `IRQ` is masked and will not generate an interrupt. If a bit is clear (0), then the corresponding `IRQ` is unmasked and can generate interrupts. The `IMR` is programmed through port 21h.

PCI Interrupts

PCI devices can share interrupts. The BIOS or operating system may assign multiple PCI devices to the same IRQ line. Any interrupt service routine (ISR) written for PCI devices must be able to handle shared interrupts. Refer to *Interrupt-Driven PC System Design* (ISBN: 0-929392-50-7) for more information on PCI interrupts.

Writing an Interrupt Service Routine (ISR)

The first step in adding interrupts to your software is to write the ISR. This is the routine that will automatically be executed each time an interrupt request occurs on the specified IRQ. An ISR is different than standard routines that you write. First, on entrance, the processor registers should be pushed onto the stack BEFORE you do anything else. Second, just before exiting your ISR, you must clear the interrupt status flag and write an end-of-interrupt command to the Intel 8259 controller. Finally, when exiting the ISR, in addition to popping all the registers you pushed on entrance, you must use the IRET instruction and not a plain RET. The IRET automatically pops the flags, CS, and IP that were pushed when the interrupt was called.

Most C compilers allow you to identify a procedure (function) as an interrupt type and will automatically add these instructions to your ISR, with one important exception: most compilers do not automatically add the end-of-interrupt command to the procedure; you must do this yourself. Other than this and the few exceptions discussed below, you can write your ISR just like any other routine. It can call other functions and procedures in your program and it can access global data. If you are writing your first ISR, RTD recommends focusing on the basics, such as incrementing a global variable.

Most operating systems have restrictions on what instructions can be called in your ISR. Consult your OS documentation for details on writing your ISR.



Note A complete explanation of interrupt programming is beyond the scope of this manual. For more information on interrupts, refer to the Appendix.

Sample Code

RTD's drivers provide examples of ISR's and interrupt handling. Refer to them as working examples. These drivers were shipped with your cpuModule, but they they can also be downloaded from RTD's website (www.rtd.com).

Watchdog Timer Control

The cpuModule includes a watchdog timer, which provides protection against programs "hanging", or getting stuck in an execution loop where they cannot respond correctly. When enabled, the watchdog timer must be periodically reset by your application program. If it is not reset before the time-out period of 1.2 seconds expires, it will cause a hardware reset of the cpuModule.

Three functions have been implemented on the cpuModule for watchdog timer control. These are:

- Watchdog timer enable
- Watchdog timer disable
- Watchdog timer refresh

To enable the watchdog timer you must write a 1 to Bit 0 of I/O register 1Eh. To ensure compatibility with future designs, you should read the register and only change the bit you need to change.

After you enable the watchdog timer, you must reset it at least once every 1.2 seconds by reading I/O 1Eh. The data read does not matter.

To disable the watchdog timer you must write a 0 to Bit 0 of I/O register 1Eh.

Enabling the watchdog timer is illustrated in the following C program fragment:

```
// Sample code to enable the watchdog timer

uint8_t temp;      // Create a variable for temporary storage

temp = inp(0x1E);  // Read in the current register value

temp = temp | 0x01; // Change the watchdog timer enable bit

outp(0x1E, temp);  // Write the modified value back to the register
```

When the watchdog timer is enabled it must be refreshed before it times out or it hardware reset the system. Refreshing the watchdog timer is illustrated in the following C program fragment:

```
// Sample code to refresh the watchdog timer
// Must do this at least once every 1.2 seconds, or the system will reboot.

inp(0x1E); // Read I/O port 0x1E to refresh
```

Disabling the watchdog timer is illustrated in the following C program fragment:

```
// Sample code to disable the watchdog timer

uint8_t temp;      // Create a variable for temporary storage

temp = inp(0x1E);  // Read in the current register value

temp = temp & 0xFE; // Change the watchdog timer enable bit

outp(0x1E, temp);  // Write the modified value back to the register
```

Real Time Clock Control

The cpuModule is equipped with a real time clock (RTC) which provides system date and time functions, and also provides 128 nonvolatile memory locations. The contents of these memory locations are retained whenever an external backup battery is connected, whether or not system power is connected.

You may access the RTC date, time, and memory using an index and data register at I/O addresses 70h and 71h. Address 70h is the Index register. It must be written with the number of the register to read or write. Refer to the map below for valid choices for the index. Data is then written to or read from the selected register by writing or reading (respectively) the data register at address 71h.



WARNING Do NOT change values stored in the RTC registers listed as RESERVED in the table below. Doing so will interfere with proper cpuModule operation.

Registers of the RTC are shown below.

Table 47 Real Time Clock Registers

Registers (hex)	Registers (decimal)	Number of Bytes	Function
00h	0	1	BCD Seconds
02h	2	1	BCD Minutes
04h	4	1	BCD Hours
06h	6	1	Day of Week
07h	7	1	Day of Month
08h	8	1	Month
09h	9	1	Year
0A–0Dh	10–13	4	RTC Control Registers
0E–31h	14–49	36	RESERVED—Do not modify!
32h	50	1	BCD Century
33–3Fh	51–63	13	RESERVED—Do not modify!
40–7Fh	64–127	64	User RAM



Note RTC access is illustrated in Application Note, SWM-64000011, which you can download from the RTD website (www.rtd.com).

Note For a detailed description of the RTC register map, refer to the data sheet for National Semiconductor's PC97317 Super I/O chip.

Parallel Port Control

The parallel port may be operated in SPP (output-only), EPP (bidirectional), and ECP (extended capabilities) modes. The mode may be selected in Setup, or by application software.

Configuring the ATA/IDE Disk Chip Socket

The cpuModule was designed to be used in embedded computing applications. In such environments, magnetic media like hard disks and floppy disks are not very desirable. It is possible to eliminate magnetic storage devices by placing your operating system and application software into the cpuModule's ATA/IDE Disk Chip socket.



WARNING Before installing a device in the ATA/IDE Disk Chip socket, the system must be configured in the correct mode. For details on configuring the socket, refer to Chapter 5, Using the cpuModule

Before installing a device in the ATA/IDE Disk Chip socket, it is highly recommend to first configure the secondary IDE controller and device mode in the BIOS setup.

The secondary IDE controller must be enabled in the BIOS to allow read and write access to the device. When a device is installed in the socket, it will always appear as a master on the cpuModule's secondary IDE controller.

From the BIOS setup screen, the user can also configure whether the socket contains a DMA mode or PIO mode device.

- **DMA Mode:** DMA mode will reduce CPU overhead. This mode can be set use multi-word DMA.
- **PIO Mode:** When the socket is in PIO mode, PIO transfers are supported. PIO Mode supports write protection.

Appendix A Hardware Reference

This appendix provides information on CMC26686CX cpuModule hardware, including:

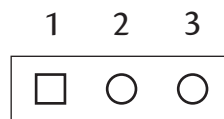
- Jumper settings and locations
- LED locations
- Mechanical dimensions
- Processor thermal management

Jumpers

Many cpuModule options are configured by positioning jumpers. Jumpers are labeled on the board as **JP** followed by a number.

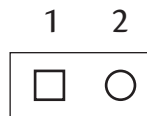
Some jumpers have three pins, allowing three settings:

- Pins 1 and 2 connected (indicated as “1–2”)
- Pins 2 and 3 connected (indicated as “2–3”)
- No pins connected



Some jumpers have two pins, allowing two settings:

- Pins 1 and 2 connected (indicated as “closed”)
- Pins 1 and 2 unconnected (indicated as “open”)



Solder jumpers are located on the cpuModule’s bottom side. Solder blobs are factory-set and rarely changed. Contact RTD Technical Support for further information.

and show the jumper and solder blob locations that are used to configure the cpuModule. In both top and bottom figures, the PC/104 bus connector is at the six o'clock position. lists the jumpers and their settings. lists the solder blobs and their settings.

Jumper and LED locations

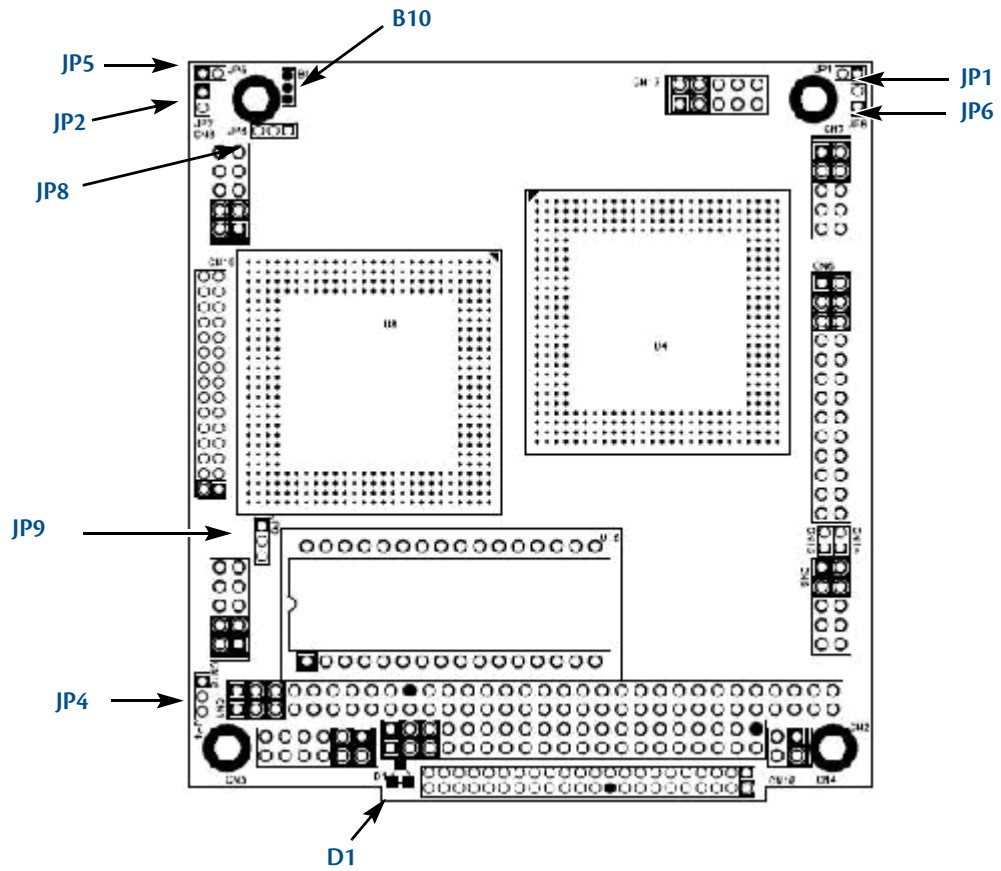


Figure 6 CMC26686CX Jumper and LED Locations (top side)

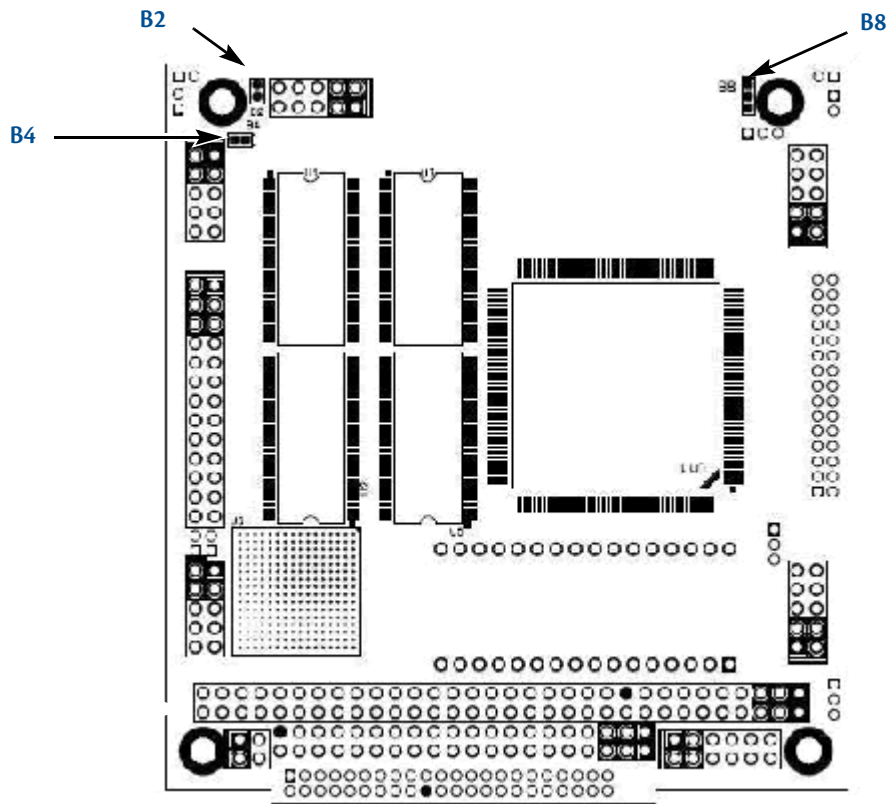


Figure 7 CMC26686CX Jumper Locations (bottom side)

Table 48 CMC26686CX Jumpers

Jumper	Pins	Function	Default
JP1	2	Enable/disable 120 Ω series termination to COM1 (CN7) in RS-422/485 modes	open
JP2	2	Enable/disable 120 Ω series termination to COM2 (CN8) in RS-422/485 modes	open
JP4	3	Select power for the ATA/IDE Disk Chip socket (U16) pins 1–2: +5V pins 2–3: +3.3V	pins 2-3
JP5	2	Install to boot to Fail Safe Boot image	open
JP6	2	<i>Factory use only</i>	open
JP8	3	Select power for the flat panel electronics pins 1–2: +3.3 V pins 2–3: +5 V	pins 1–2
JP9	3	Select power for flat panel backlight pins 1–2: +12 V pins 2–3: +5 V	pins 2–3

Table 49 CMC26686CX Solder Blobs

Solder Blob	Positions	Function	Default
B2	2	Solder closed to connect USB ground to frame ground	open
B4	2	Solder closed to connect frame ground to digital ground	open
B8	3	<i>Factory use only</i>	pins 2-3
B10	3	<i>Factory use only</i>	pins 1-2

Table 50 CMC26686CX LEDs

LED	Function (color)	Description
D1	Onboard IDE Activity (red)	Indicates drive activity on the primary IDE connector (CN10) or on the ATA/IDE Disk Chip socket (U16).

Physical Dimensions

Figure 8 shows the mechanical dimensions of the CMC26686CX cpuModule (in inches).

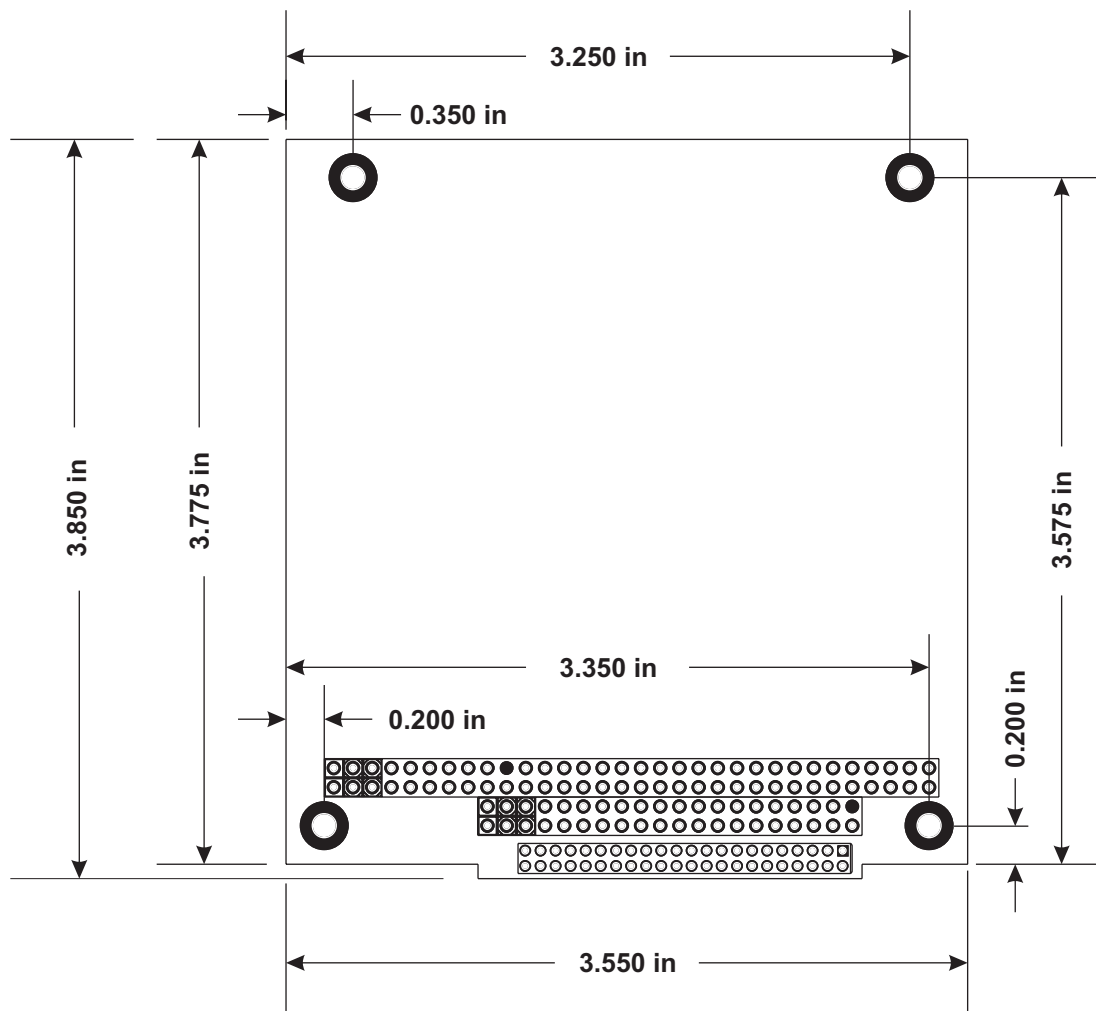


Figure 8 CMC26686CX Physical Dimensions (± 0.005 inches)

Processor Thermal Management

The industrial grade processor IC of the cpuModule must receive adequate cooling to ensure proper operation and good reliability. The ambient temperature of the processor must not exceed +85°C. The processor is therefore supplied with an attached fan or heat sink with a thermal resistance of 5° C/W.



Note This cpuModule is not warranted against damage caused by overheating due to improper or insufficient heatsinking or airflow.

Table 51 shows the required airflow in linear feet per minute (LFM).

Table 51 Processor Thermal Management

Ambient Temperature +85°C		Airflow Approach Velocity (LFM)						
Part Number	Frequency	25° C	35° C	45° C	55° C	65° C	75° C	85° C
CMC26686CX300	300 MHz	0	0	25	25	50	100	400
CMC26686CX333	333 MHz	0	25	25	50	100	250	700



Appendix B Troubleshooting

Many problems you may encounter with operation of your CMC26686CX cpuModule are due to common errors. This appendix includes the following sections to help you get your system operating properly.

- Common problems and solutions
- Troubleshooting a PC/104 system
- How to obtain technical support

Common Problems and Solutions

Table 52 lists some of the common problems you may encounter while using your CMC26686CX cpuModule, and suggests possible solutions.

If you are having problems with your cpuModule, review this table before contacting RTD Technical Support.

Table 52 Troubleshooting

Problem	Cause	Solution
cpuModule "will not boot"	no power or wrong polarity	<ul style="list-style-type: none"> check for correct power on PC/104 bus connectors
	incorrect Setup	<ul style="list-style-type: none"> reboot and press Delete to run Setup
	defective or misconnected device on bus	<ul style="list-style-type: none"> check for misaligned bus connectors remove other cards from stack
	cable connected backwards	<ul style="list-style-type: none"> verify all cables are connected correctly
	SSD device installed backwards	<ul style="list-style-type: none"> check for an SSD device installed in socket backwards
cpuModule keeps rebooting	problem with power supply	<ul style="list-style-type: none"> check for correct power on PC/104 bus connector
	reset switch is on	<ul style="list-style-type: none"> check that the reset button is not pushed in
	watchdog timer is not being serviced quickly enough	<ul style="list-style-type: none"> verify that the watchdog timer is being refreshed before it times out
cpuModule will not boot from particular drive or device	device not bootable	<ul style="list-style-type: none"> use <code>sys</code> command on drive or reformat the device using the <code>/s</code> switch
	device not formatted	<ul style="list-style-type: none"> format drive using <code>/s</code> switch
	power not connected to boot drive	<ul style="list-style-type: none"> connect power cable to floppy or hard drive
Atmel Flash shows disk space available, but it cannot be written	part smaller than 1.44 MB was formatted as 1.44 MB; will show space available even when full	<ul style="list-style-type: none"> ignore "disk space remaining" messages from DOS REMEMBER! A bootable disk contains 3 hidden files plus format information, totaling about 150 KB

Table 52 Troubleshooting (cont'd)

Problem	Cause	Solution
erratic operation	excessive bus loading	<ul style="list-style-type: none"> • reduce number of PC/104 modules in stack • remove termination components from bus signals • remove any power supply bus terminations
	power supply noise	<ul style="list-style-type: none"> • examine power supply output with oscilloscope • glitches below 4.75 VDC will trigger a reset • add bypass caps
	power supply limiting	<ul style="list-style-type: none"> • examine power supply output with oscilloscope • check for voltage drop below 4.75 VDC when hard drive or floppy drive starts • add bypass caps
	insufficient cabling through power connector	<ul style="list-style-type: none"> • increase wire gauge to connector • power through bus connectors
	temperature too high	<ul style="list-style-type: none"> • add fan, processor heatsink, or other cooling device(s) • See <i>Processor Thermal Management</i> on page 82
	memory address conflict	<ul style="list-style-type: none"> • check for two hardware devices (e.g. Ethernet, SSD, Arcnet, PCMCIA) trying to use the same memory address • check for two software devices (e.g. EMM386, PCMCIA drivers, etc.) trying to use the same memory addresses • check for hardware and software devices trying to use the same memory address • check for an address range shadowed (see Advanced Setup screen) while in use by another hardware or software device
	I/O address conflict	<ul style="list-style-type: none"> • check for another module trying to use I/O addresses reserved for the cpuModule between 010h and 01Fh • check for two modules (e.g. dataModules, PCMCIA cards, Ethernet) trying to use the same I/O addresses
keyboard does not work	keyboard interface damaged by misconnection	<ul style="list-style-type: none"> • check if keyboard LEDs light
	wrong keyboard type	<ul style="list-style-type: none"> • verify keyboard is an "AT" type or switch to "AT" mode
floppy drive light always on	cable misconnected	<ul style="list-style-type: none"> • check for floppy drive cable connected backwards
two hard drives will not work, but one does	both drives configured for master	<ul style="list-style-type: none"> • set one drive for master and the other for slave operation (consult drive documentation)
floppy does not work	"data error" due to drive upside down	<ul style="list-style-type: none"> • orient drive properly (upright or on side)
will not boot when video card is removed	illegal calls to video controller	<ul style="list-style-type: none"> • look for software trying to access nonexistent video controller for video, sound, or beep commands
abnormal video	flat panel is enabled	<ul style="list-style-type: none"> • disable the flat panel in the BIOS
can only use 640 x 480 resolution in Windows	flat panel is enabled	<ul style="list-style-type: none"> • disable the flat panel in the BIOS
	video drivers not installed	<ul style="list-style-type: none"> • install the video drivers
will not boot from PCMCIA hard drive	booting from PCMCIA is not supported	<ul style="list-style-type: none"> • boot from SSD, use autoexec.bat to load PCMCIA drivers, run application from PCMCIA card
COM port will not work in RS-422 or RS-485 modes	not configured for RS-422/485	<ul style="list-style-type: none"> • correctly configure serial port in Setup program
COM port will not transmit in RS-422 or RS-485 mode	not enabling transmitters	<ul style="list-style-type: none"> • control RTS* bit of Modem Control Register to enable transmitters; see Serial Port descriptions
date and time not saved when power is off	no backup battery	<ul style="list-style-type: none"> • connect a backup battery to the multi-function connector

Table 52 Troubleshooting (cont'd)

Problem	Cause	Solution
cannot enter BIOS	quick boot enabled with no hard drives	<ul style="list-style-type: none">• install JP5, reboot, and run qboot.exe and reboot.

Troubleshooting a PC/104 System

If you have reviewed the preceding table and still cannot isolate the problem with your CMC26686CX cpuModule, please try the following troubleshooting steps. Even if the resulting information does not help you find the problem, it will be very helpful if you need to contact technical support.

1. **Simplify the system.** Remove items one at a time and see if one particular item seems to cause the problem.
2. **Swap components.** Try replacing items in the system one-at-a-time with similar items.

How to Obtain Technical Support

If after following the above steps, you still cannot resolve a problem with your CMC26686CX cpuModule, please gather the following information:

- cpuModule model, BIOS version, and serial number
- List of all boards in system
- List of settings from cpuModule Setup program
- Printout of autoexec.bat and config.sys files (if applicable)
- Description of problem
- Circumstances under which problem occurs

Then contact RTD Technical Support:

Phone: 814-234-8087

Fax: 814-234-5218

E-mail: techsupport@rtd.com

Appendix C IDAN™ Dimensions and Pinout

cpuModules, like all other RTD PC/PCI-104 modules, can be packaged in Intelligent Data Acquisition Node (IDAN) frames, which are milled aluminum frames with integrated heat sinks and heat pipes for fanless operation. RTD modules installed in IDAN frames are called building blocks. IDAN building blocks maintain the simple but rugged PC/104 stacking concept. Each RTD module is mounted in its own IDAN frame and all I/O connections are brought to the walls of each frame using standard PC connectors. No connections are made from module to module internal to the system other than through the PC/104 and PC/104-Plus bus, enabling quick interchangeability and system expansion without hours of rewiring and board redesign.

The CMC26686CX cpuModule can also be purchased as part of a custom-built RTD HiDAN™ or HiDANplus™ High Reliability Intelligent Data Acquisition Node. This appendix provides the dimensions and pinouts of the CMC26686CX installed in an IDAN frame. Contact RTD for more information on high reliability IDAN, HiDAN, and HiDANplus PC/PCI-104 systems.



IDAN—Adhering to the PC/104 stacking concept, IDAN allows you to build a customized system with any combination of RTD modules.

IDAN Heat Pipes—Advanced heat pipe technology maximizes heat transfer to heat sink fins.



HiDANplus—Integrating the modularity of IDAN with the ruggedization of HiDAN, HiDANplus enables connectors on all system frames, with signals running between frames through a dedicated stack-through raceway.

IDAN Dimensions and Connectors

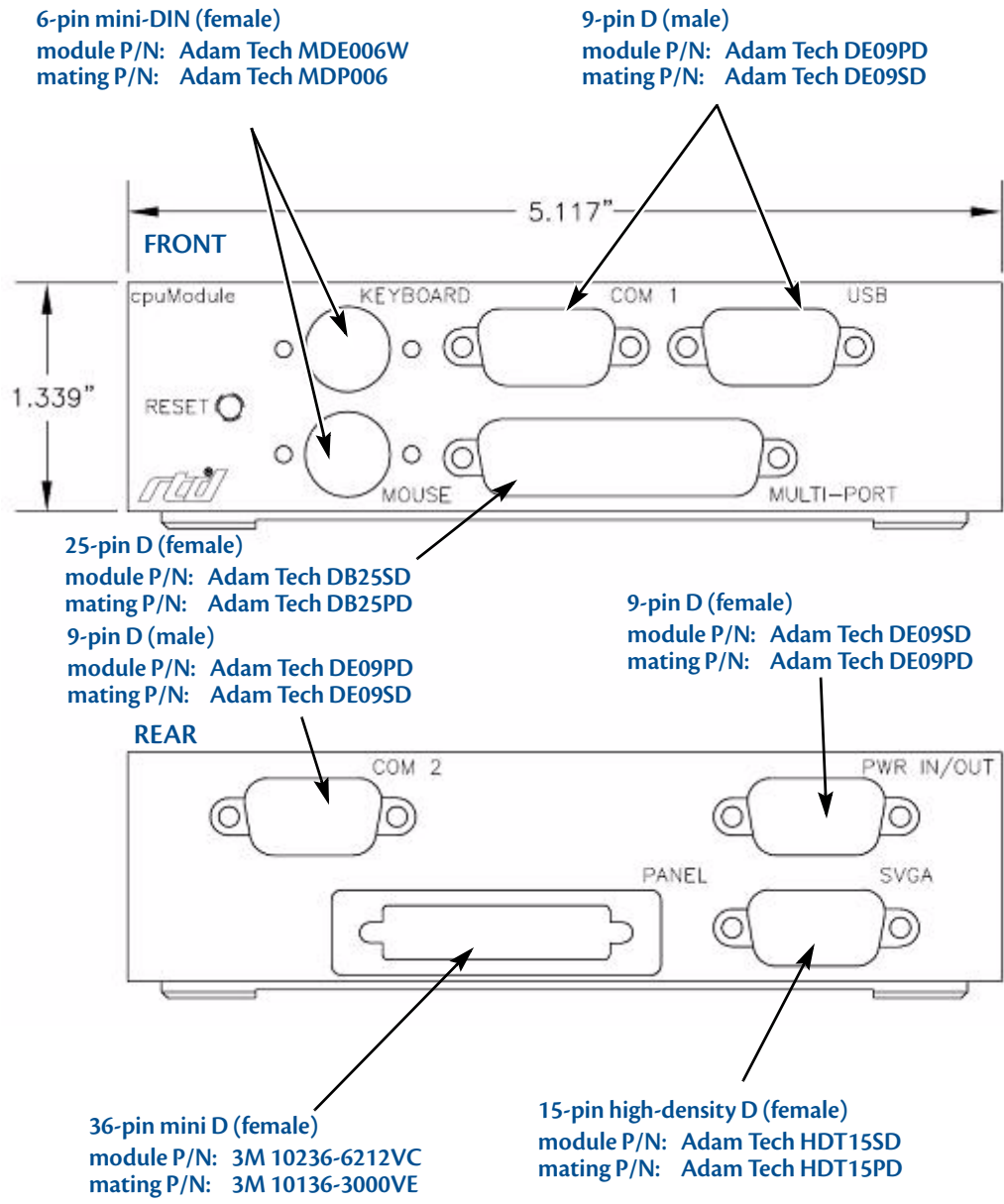


Figure 9 IDAN-CMC26686CX Connectors

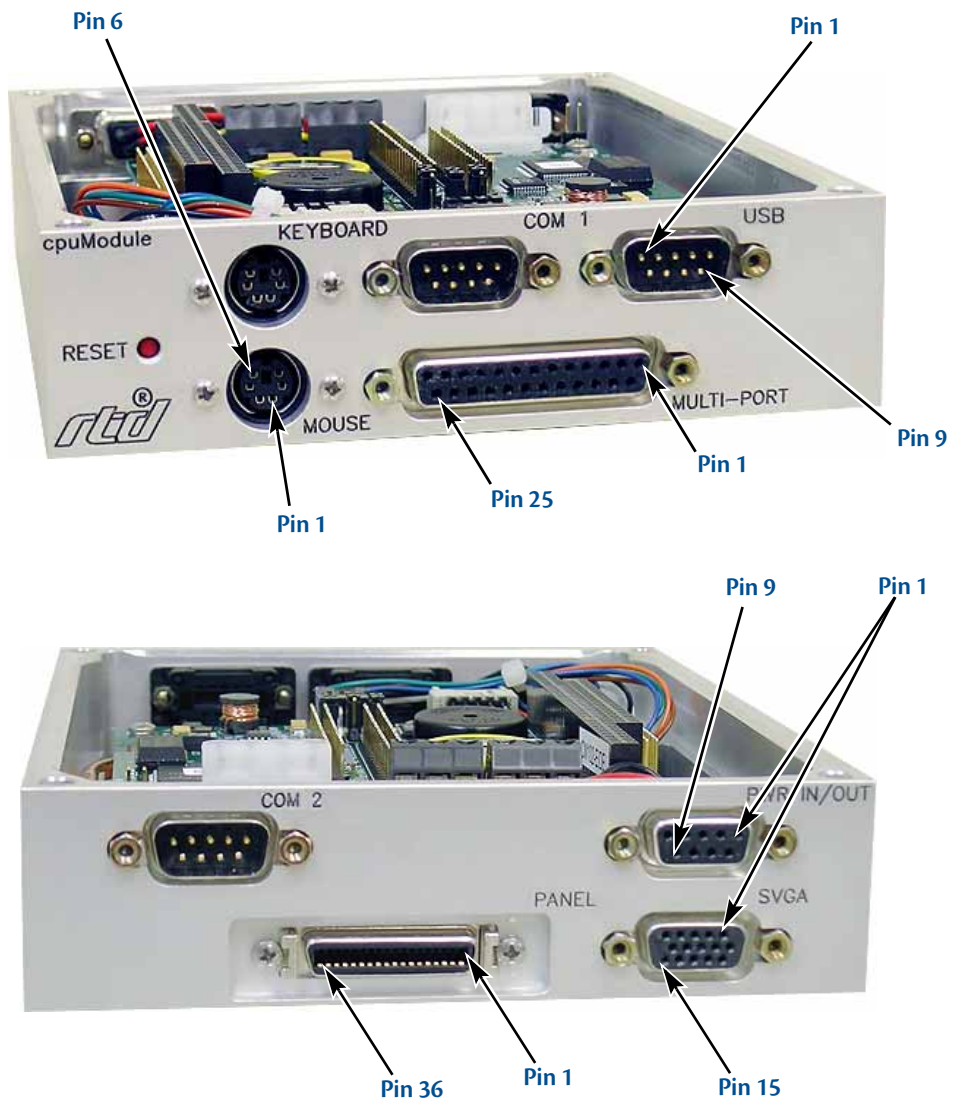


Figure 10 IDAN-CMC26686CX Connector Pins

External I/O Connections

Table 53 Power In/Out—9-Pin D Connector (female)

IDAN Pin #	Signal
1	+5 V
2	Ground
3	+12 V
4	Ground
5	-12 V
6	+5 V
7	Ground
8	Reserved
9	Reserved

Table 54 PS/2 Mouse—6-Pin mini-DIN Connector (female)

IDAN Pin #	Signal	Function
1	MDAT	Mouse Data
2	Reserved	—
3	GND	Ground
4	+5 V	+5 Volts
5	MCLK	Mouse Clock
6	Reserved	—

Table 55 Keyboard—6-Pin mini-DIN Connector (female)

IDAN Pin #	Signal	Function
1	KDAT	Keyboard Data
2	Reserved	—
3	GND	Keyboard Ground
4	+5 V	+5 V
5	KCLK	Keyboard Clock
6	Reserved	—

Table 56 COM1/COM2 (RS-232)—9-Pin D Connector (male)

IDAN Pin #	Signal	Function	Mode
1	DCD	Data Carrier Detect	Input
2	RXD	Receive Data	Input
3	TXD	Transmit Data	Output
4	DTR	Data Terminal Ready	Output
5	GND	Ground	—
6	DSR	Data Set Ready	Input
7	RTS	Request To Send	Output
8	CTS	Clear To Send	Input
9	RI	Ring Indicator	Input

Table 57 COM1/COM2 (RS-422/485)—9-Pin D Connector (male)

IDAN Pin #	Signal	Function	Mode
1	Reserved	—	—
2	RXD-	Receive Data -	Input
3	TXD-	Transmit Data -	Output
4	Reserved	—	—
5	GND	Ground	—
6	Reserved	—	—
7	TXD+	Transmit Data +	Output
8	RXD+	Receive Data +	Input
9	Reserved	—	—

Table 58 multiPort—25-Pin D Connector (female)

IDAN Pin #	aDIO Port	Parallel Port	Floppy Port	CPU Pin #
1	strobe 0	STB	—	1
2	P1-0	PD0	INDEX#	3
3	P1-1	PD1	TRK0#	5
4	P1-2	PD2	WRTPRT#	7
5	P1-3	PD3	RDATA#	9
6	P1-4	PD4	DSKCHG	11
7	P1-5	PD5	—	13
8	P1-6	PD6	—	15
9	P1-7	PD7	—	17
10	P0-0	ACK	DS1#	19
11	P0-1	BSY	MTR#	21
12	P0-2	PE	WDATA#	23
13	P0-3	SLCT	WGATE#	25
14	P0-4	AFD	DR0#	2
15	P0-5	ERR	HDSEL#	4
16	P0-6	INIT	DIR#	6
17	P0-7	SLIN	STEP#	8
18	strobe 1	GND	GND	10
19	GND	GND	GND	12
20	GND	GND	GND	14
21	GND	GND	GND	16
22	GND	GND	GND	18
23	GND	GND	GND	20
24	GND	GND	GND	22
25	GND	GND	GND	24

Table 59 Panel—36-Pin mini D Connector (female)

IDAN Pin #	Signal	Function	CPU Pin #
1	FP_VCC	Power for flat panel electronics	1
2	FP_VDDEN	Enable for flat panel power	3
3	GND	Ground	5
4	GND	Ground	7
5	GP_VSYNC	Vertical Sync	9
6	FP_CLK	Clock	11
7	FP_BLUE0	Blue bit 0 (LSB)	13
8	FP_BLUE2	Blue bit 2	15
9	FP_BLUE4	Blue bit 4	17
10	FP_GREEN0	Green bit 0 (LSB)	19
11	FP_GREEN2	Green bit 2	21
12	FP_GREEN4	Green bit 4	23
13	FP_RED0	Red bit 0 (LSB)	25
14	FP_RED2	Red bit 2	27
15	FP_RED4	Red bit 4	29
16	—	Reserved	—
17	—	Reserved	—
18	—	Reserved	—
19	FP_VBKLT	Power for flat panel backlight	2
20	FP_ENABLK	Enable for Backlight Power	4
21	FP_DISPEN	Display Enable	6
22	FP_HSYNC	Horizontal Sync	8
23	GND	Ground	10
24	GND	Ground	12
25	FP_BLUE1	Blue bit 1	14
26	FP_BLUE3	Blue bit 3	16
27	FP_BLUE5	Blue bit 5	18
28	FP_GREEN1	Green bit 1	20
29	FP_GREEN3	Green bit 3	22
30	FP_GREEN5	Green bit 5	24
31	FP_RED1	Red bit 1	26
32	FP_RED3	Red bit 3	28
33	FP_RED5	Red bit 5	30
34	—	Reserved	—
35	—	Reserved	—
36	—	Reserved	—

Table 60 SVGA—15-Pin High Density D Connector (female)

IDAN Pin #	Signal	Function	CPU Pin #
1	Red	Red Analog Output	4
2	Green	Green Analog Output	6
3	Blue	Blue Analog Output	8
4	Reserved	Reserved	—
5	GND	Ground	9
6	GND	Ground	9
7	GND	Ground	9
8	GND	Ground	10
9	+5 VDC	Reserved	7
10	GND	Ground	10
11	Reserved	Reserved	—
12	DDC Data	Monitor data	5
13	HSYNC	Horizontal Sync	2
14	VSYNC	Vertical Sync	1
15	DDC CLK	Monitor Clock	3

Table 61 USB—9-Pin D Connector (male)

IDAN Pin #	Signal	Function	Mode
1	VCC1	Supply +5 V to USB1	output
2	Data USB1–	USB1 Data–	input/output
3	Data USB1+	USB1 Data+	input/output
4	GND	Ground	—
5	GND	Ground	—
6	VCC2	Supply +5 V to USB2	output
7	Data USB2–	USB2 Data–	input/output
8	Data USB2+	USB2 Data+	input/output
9	GND	Ground	—



Appendix D Additional Information

Application Notes

RTD offers many application notes that provide assistance with the unique feature set of the Geode cpuModule. For the latest application notes, refer to the RTD website.

Drivers and Example Programs

To obtain the latest versions of drivers and example programs for this cpuModule, refer to the RTD website.

Interrupt Programming

For more information about interrupts and writing interrupt service routines, refer to the following book:

Interrupt-Driven PC System Design
by Joseph McGivern
ISBN: 0929392507

Serial Port Programming

For more information about programming serial port UARTs, consult the following book:

Serial Communications Developer's Guide
by Mark Nielson
ISBN: 0764545701

PC/104 and PC/104-Plus Specifications

A copy of the latest PC/104 and PC/104-Plus specifications can be found on the webpage for the PC/104 Embedded Consortium:

<http://www.pc104.org>



Appendix E Limited Warranty

RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD Embedded Technologies, Inc. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, RTD Embedded Technologies will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to RTD Embedded Technologies. All replaced parts and products become the property of RTD Embedded Technologies. Before returning any product for repair, customers are required to contact the factory for a Return Material Authorization number.

This limited warranty does not extend to any products which have been damaged as a result of accident, misuse, abuse (such as: use of incorrect input voltages, improper or insufficient ventilation, failure to follow the operating instructions that are provided by RTD Embedded Technologies, "acts of god" or other contingencies beyond the control of RTD Embedded Technologies), or as a result of service or modification by anyone other than RTD Embedded Technologies. Except as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranties of merchantability and fitness for a particular purpose, and RTD Embedded Technologies expressly disclaims all warranties not stated herein. All implied warranties, including implied warranties for merchantability and fitness for a particular purpose, are limited to the duration of this warranty. In the event the product is not free from defects as warranted above, the purchaser's sole remedy shall be repair or replacement as provided above. Under no circumstances will RTD Embedded Technologies be liable to the purchaser or any user for any damages, including any incidental or consequential damages, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

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This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

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