# DM35418HR/DM35218HR

*PCI Express Data Acquisition Board*

## User's Manual

BDM-610010041 Rev H

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*AS9100 and ISO 9001 Certified*

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# Revision History

| | |
|---|---|
| Rev A | Initial Release |
| Rev B | Added DM35218 information, updated 68-pin IDAN connector pin out |
| Rev C | Updated 62-Pin IDAN connector pin out, changed all reference of A/D to ADC, changed all reference of D/A to DAC |
| Rev D | Added Section 3.3.5 LEDs<br>CN5 was removed from factory use only<br>Removed generic text from sections 6.3.17 and 6.4.16<br>Removed gain from ADC voltage formula<br>Removed Note from sections 6.3.17 and 6.4.16<br>Added table to section 6.4.16<br>CN3's 3.3V load capability added to section 2.2<br>Add Clock Source description<br>Added CHn_FIFO_DATA_CNT register description to ADC and DAC Functional Blocks<br>Updated IDAN dimension drawing<br>Updated FFT Specifications |
| Rev E | ~~40 MHz system clock frequency specified in section 6.1.7~~<br>In the digital IO section of Table 3, the symbols for the Input High Voltage and Input Low Voltage were swapped. |
| Rev F | Changed formatting to Section 6<br>Added sections Temperature Sensor, Digital I/O and Functional Characteristics<br>Updated power consumption |
| Rev G | Added Pinouts for both the DM35418 and DM35218<br>Added pin position table for board connectors<br>Added IDAN pin number indicators to connectors |
| Rev H | Changed all references of CLK_SRC_GBL to CLK_BUS |

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# 1 Introduction

## 1.1 Product Overview

The DM35418 is a software configurable high-speed, 18-bit data acquisition module in the PCIe/104 format. This module provides 8 differential or single-ended analog input channels, with programmable gain and input ranges. This module is capable of either independent or simultaneous sampling. The DM35418 also features eight 16-bit high-speed analog outputs with programmable output ranges, and a 32-bit port of digital I/O, and synchronization of multiple boards with the SyncBus.

The DM35218 is a software configurable high-speed, 18-bit data acquisition module in the PCIe/104 format. This module provides 4 differential or single-ended analog input channels, with programmable gain and input ranges. This module is capable of either independent or simultaneous sampling. The DM35218 also features four 16-bit high-speed analog outputs with programmable output ranges, and a 32-bit port of digital I/O, and synchronization of multiple boards with the SyncBus.

## 1.2 Board Features

- PCI Express Bus:
  - PCIe/104 Universal Board
    - Interfaces with Type 1 or Type 2 bus
    - Lane repopulation allows maximum system expansion
  - Provides 2.5 Gbps in each direction
  - In-band interrupts and messages
  - Message Signaled Interrupt (MSI) support
- Analog inputs:
  - 4/8 channels, high-speed inputs with *independent* sampling, or *simultaneous* sampling
  - 1.538 MSPS maximum input sampling rate
  - 18-bit resolution
  - Programmable single ended or differential inputs per channels
  - Programmable input full-scale ranges in bipolar mode: ±10V, ±5V, ±2.5V, ±1.25V, ±0.625V,
  - Programmable input full-scale ranges in unipolar mode: 0-10V, 0-5V, 0-2.5V 0-1.25V
  - Sampling modes and triggers are configurable independently
  - Threshold detection can generate an interrupt, or be used as a start or stop trigger
  - Configurable IIR filter on each channel
- Analog outputs:
  - 4/8 channels high-speed
  - 16-bit D/A converters
  - MSPS maximum update rate
  - Output full-scale ranges: ±2.5V, ±5V, ±10V
- SyncBus
  - Allows synchronization of the sampling clock on multiple boards
  - Allows synchronization of start and stop triggers on multiple boards
  - Software selectable Master/Slave
  - Software selectable termination
- Digital I/O
  - 32-bit port of digital I/O
  - Bit programmable direction
  - 5V Tolerant TTL Signaling level

## 1.3 Ordering Information

The DM35418HR/DM35218HR is available with the following options:

***Table 1: Ordering Options***

| Part Number | Description |
|---|---|
| DM35418HR | PCIe/104 Analog I/O dataModule |
| DM35218HR | PCIe/104 Analog I/O dataModule |
| IDAN-DM35418HR-62S | PCIe/104 Analog I/O dataModule in IDAN enclosure with 62-pin D-Sub Connector |
| IDAN-DM35218HR-62S | PCIe/104 Analog I/O dataModule in IDAN enclosure with 62-pin D-Sub Connector |

*Table 1: Ordering Options*

| Part Number | Description |
|---|---|
| IDAN-DM35418HR-68S | PCIe/104 Analog I/O dataModule in IDAN enclosure with 68-pin High-Density Connector |
| IDAN-DM35218HR-68S | PCIe/104 Analog I/O dataModule in IDAN enclosure with 68-pin High-Density Connector |

The Intelligent Data Acquisition Node (IDAN®) building block can be used in just about any combination with other IDAN building blocks to create a simple but rugged 104™ stack. This module can also be incorporated in a custom-built RTD HiDAN® or HiDANplus® High Reliability Intelligent Data Acquisition Node. Contact RTD sales for more information on our high reliability systems.

## 1.4 Contact Information

### 1.4.1 Sales Support

For sales inquiries, you can contact RTD Embedded Technologies sales via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: sales@rtd.com

### 1.4.2 Technical Support

If you are having problems with your system, please try the steps in the Troubleshooting section of this manual on page 57.

For help with this product, or any other product made by RTD, you can contact RTD Embedded Technologies technical support via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: techsupport@rtd.com

# 2 Specifications

## 2.1 Operating Conditions

*Table 2: Operating Conditions*

| Symbol | Parameter | Test Condition | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{cc5}$ | 5V Supply Voltage | | | 4.75 | 5.25 | V |
| $V_{cc3}$ | 3.3V Supply Voltage | | | n/a | n/a | V |
| $V_{cc12}$ | 12V Supply Voltage | | | n/a | n/a | V |
| $V_{cc-12}$ | -12V Supply Voltage | | | n/a | n/a | V |
| $T_a$ | Operating Temperature | | | -40 | +85 | C |
| $T_s$ | Storage Temperature | | | -55 | +125 | C |
| RH | Relative Humidity | Non-Condensing | | 0 | 90% | % |
| MTBF | Mean Time Before Failure | Telcordia Issue 2 30°C, Ground benign, controlled | DM35418HR | 970,115 | | Hours |
| | | | DM35218HR | 1,106,548 | | Hours |

## 2.2 Electrical Characteristics

*Table 3: Electrical Characteristics*

| Symbol | Parameter | Test Condition | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| P | Power Consumption[1] | DM35418HR: $V_{cc5}$ = 5.0V | | 8.85 | | W |
| | | DM35218HR: $V_{cc5}$ = 5.0V | | 5.9 | | W |
| $I_{cc5}$ | 5V Input Supply Current | DM35418HR: Active | | 1.77 | | A |
| | | DM35218HR: Active | | 1.18 | | A |
| PCIe/104 Bus | | | | | | |
| | Differential Output Voltage | | 0.8 | | 1.2 | V |
| | DC Differential TX Impedance | | 80 | | 120 | Ω |
| | Differential Input Voltage | | 0.175 | | 1.2 | V |
| | DC Differential RX Impedance | | 80 | | 120 | Ω |
| | Electrical Idle Detect Threshold | | 65 | | 175 | mV |
| Analog to Digital Converter | | | | | | |
| | Linear Input Voltage | IN+ or IN - | -10 | | 10 | V |
| FSR | Full-scale Differential Input Voltage | $V_{IN}$ = (IN+ - IN-)<br>G = PGA Gain | $\frac{-5}{G}$ | | $\frac{4.99996}{G}$ | V |
| | Resolution | | | | 18 | Bits |
| | Data Rate | | | | 1.5385 | MSPS |
| | Input Impedance | | | | 1.25 | MΩ |
| | ENOB | Input = 0.5dBFS @ 10kHz Differential Inputs, ±10V | | 15.03 | | Bits |
| | SNR | Input = 0.5dBFS @ 10kHz Differential Inputs, ±10V | | 92.24 | | dB |
| | SINAD | Input = 0.5dBFS @ 10kHz Differential Inputs, ±10V | | 81.83 | | dB |
| | THD | Input = 0.5dBFS @ 10kHz Differential Inputs, ±10V | | -82.19 | | dB |
| | SFDR | Input = 0.5dBFS @ 10kHz Differential Inputs, ±10V | | 92.19 | | dB |
| | Third Order Intermodulation | Input = Combination of 10Khz @ -8dB and 11Khz @ -8dB | | 83.36 | | dB |
| | Noise Free Bits | Inputs Grounded Differential Inputs, ±10V | | 14.19 | | Bits |
| G | Gains | | | | 0.5,1,2,4,8 | |
| Digital to Analog Converter | | | | | | |
| | Full-scale Analog Output Voltage | G=1 | -2.5 | | +2.49998 | V |
| | Resolution | | | | 16 | Bits |
| INL | Relative Accuracy | | | | ±2 | LSB |

*Table 3: Electrical Characteristics*

| Symbol | Parameter | Test Condition | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| | Gain Error | | | | ±3 | LSB |
| | Settling Time | | | | 2 | µs |
| | Output Current | | | | 5 | mA |
| | -3dB Frequency | | | | 2.2 | MHz |
| | Slew Rate | | | | 17 | V/µs |
| G | Gains | | | | 1,2,4 | |
| Digital I/O (LVTTL) | | | | | | |
| $V_{IL}$ | Input High Voltage | | 2.0 | | 3.3 | V |
| $V_{IL}$ | Input Low Voltage | | -0.5 | | 0.8 | V |
| $V_{OL}$ | Output Low Voltage | $I_O$ =-12mA | 0 | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_O$ = -12mA | 2.4 | | 3.3 | V |
| | 3.3V Output | CN3 | | | 100 | mA |
| SyncBus (LVDS) | | | | | | |
| | Differential Input Voltage | | | | 2.4 | V |
| | Input Voltage Threshold | | -0.05 | | 0.05 | V |
| | Differential Output Voltage | $I_O$ = -4µA | 0.480 | | 0.650 | V |
| | Common Mode Output Voltage | $I_O$ =-20µA | 0.3 | | 2.1 | V |

[1] Measured running ADC continuous DMA example. All channels sampling at max rate and DAC outputs were looped back to ADC inputs.

## 2.1 Functional Characteristics

*Table 4: Functional Characteristics*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| GBC_SYS_CLK_FREQ | System Clock Frequency | 40 | MHz |
| | Analog to Digital FIFO Size | 511 | D-Words |
| | Digital to Analog FIFO Size | 511 | D-Words |

### 2.1.1 ANALOG INPUT FFT PLOTS

In Figure 1, a coherent 10kHz sine wave signal was attached to input Channel 0 in the +/-10V, Differential mode. The FFT absolute value was calculated using a Blackman-Hanning three term window.

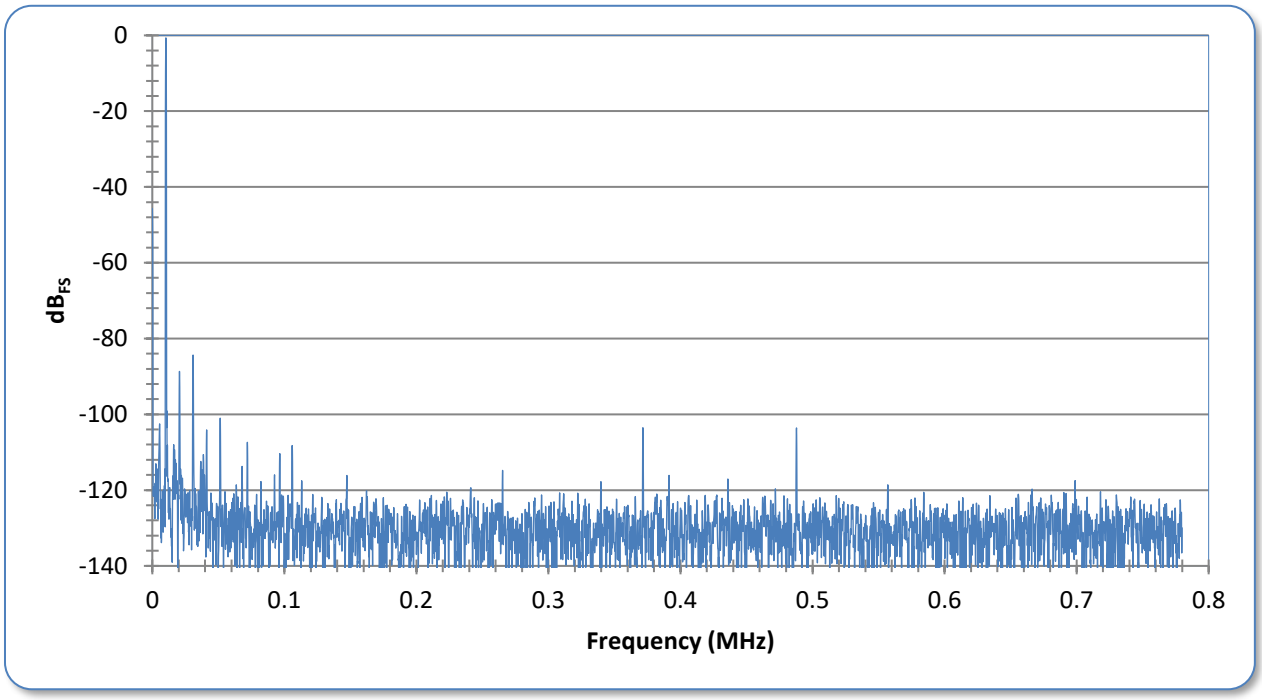



*Figure 1: Channel FFT*

### 2.1.2 ANALOG INPUT HISTOGRAMS

In Figure 2 you can see a histogram of samples from sampling a grounded input in +/-10 V, differential input range. The number of samples is 131072.

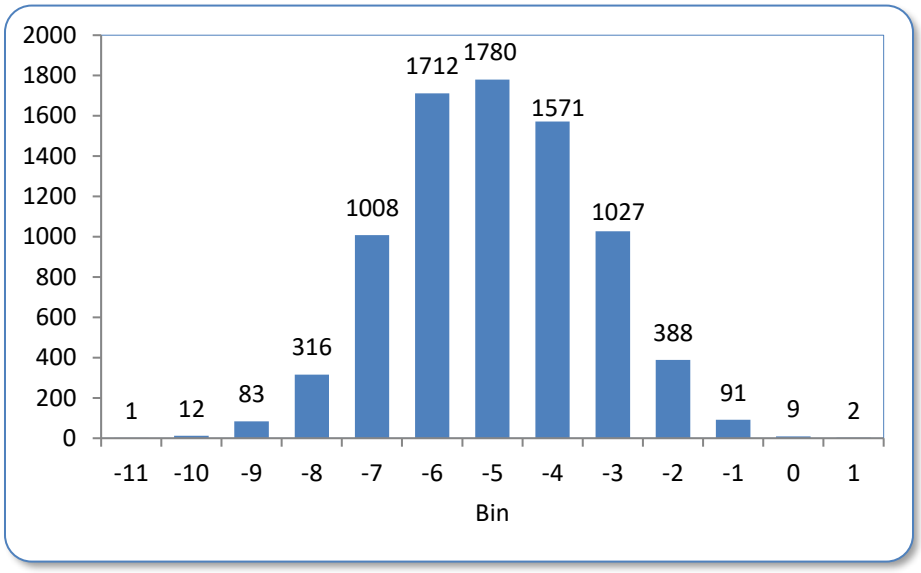



*Figure 2: Histogram*

# 3 Board Connection

## 3.1 Board Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your board in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the board at the edges, and do not touch the components or connectors. Handle the board in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

## 3.2 Physical Characteristics

STEP model is available upon request; contact RTD Tech Support for more information.

- Weight: Approximately 99.8 g (0.22 lbs) with heatsink
- Dimensions: 90.17 mm L x 95.89 mm W (3.550 in L x 3.775 in W)

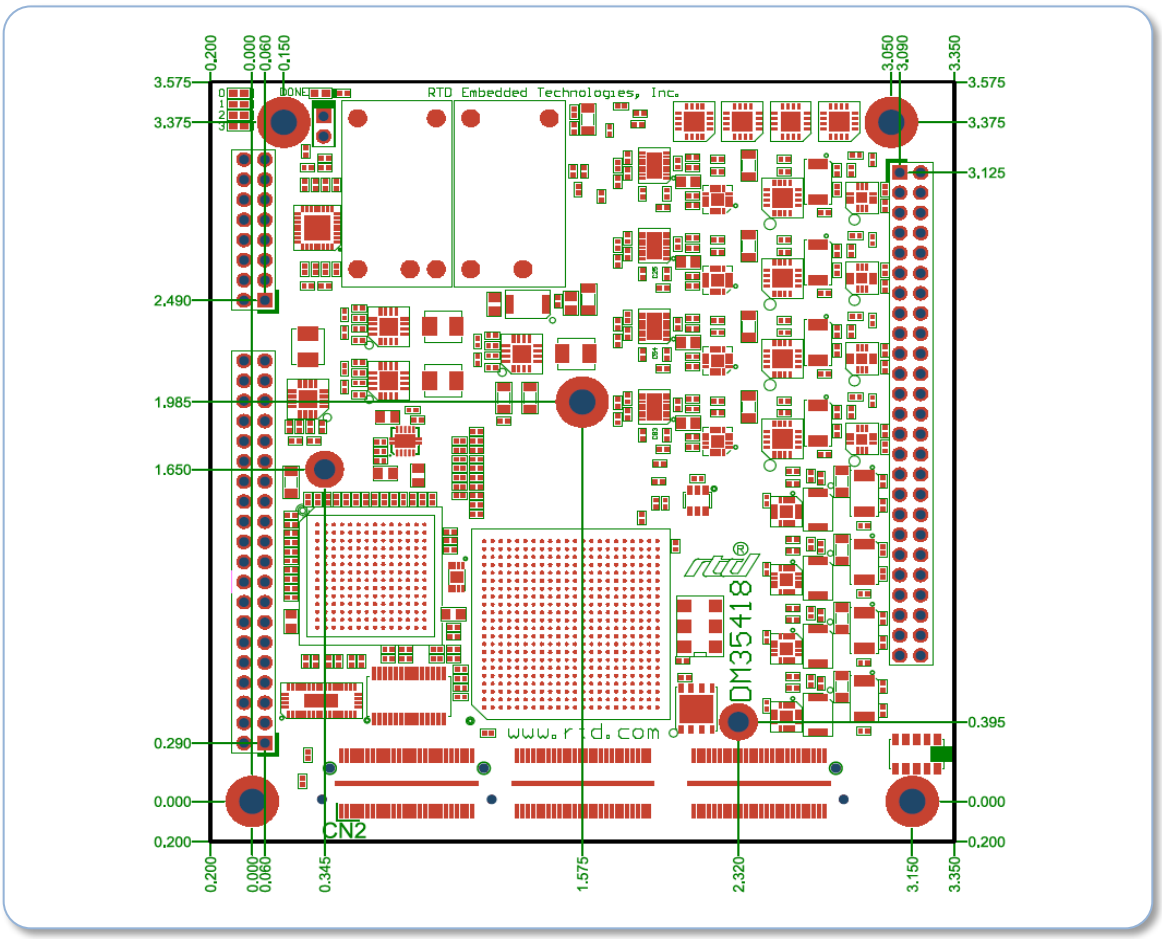



***Figure 3: Board Dimensions***

## 3.3 Connectors and Jumpers

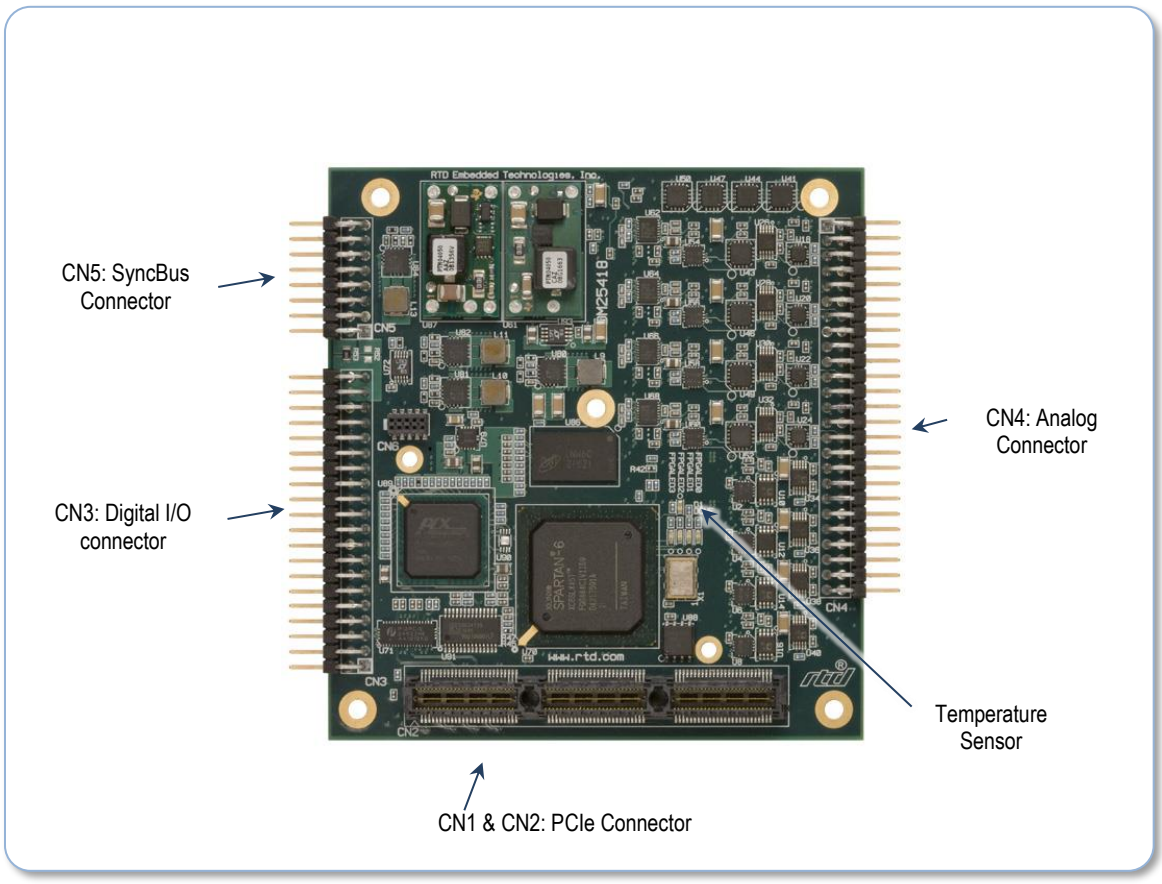



***Figure 4: Board Connections***

### 3.3.1 Bus Connectors

#### CN1(Top) & CN2(Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the PCI/104-Express Specification. (See PC/104 Specifications on page 58)

The DM35418HR/DM35218HR is a “Universal” board, and can connect to either a Type 1 or Type 2 PCIe/104 connector.

### 3.3.2 DM35418 External I/O Connectors

#### CN3: Digital I/O Connector

The Digital I/O Connector is a 2 x 20, 0.1" spacing right-angle connector. The pin assignments are shown in Table 5 below. A typical mating connector is a FCI 65043-017LF. Pin 1 is indicated by a square solder pad.

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin 39 | Pin 37 | Pin 35 | Pin 33 | Pin 31 | Pin 29 | Pin 27 | Pin 25 | Pin 23 | Pin 21 | Pin 19 | Pin 17 | Pin 15 | Pin 13 | Pin 11 | Pin 9 | Pin 7 | Pin 5 | Pin 3 | **Pin 1** |
| Pin 40 | Pin 38 | Pin 36 | Pin 34 | Pin 32 | Pin 30 | Pin 28 | Pin 26 | Pin 24 | Pin 22 | Pin 20 | Pin 18 | Pin 16 | Pin 14 | Pin 12 | Pin 10 | Pin 8 | Pin 6 | Pin 4 | Pin 2 |

***Table 5: CN3 Single-Ended Mode Pin-out***

| | | | |
|---|---|---|---|
| DIO0.1 | 2 | 1 | DIO0.0 |
| DIO0.3 | 4 | 3 | DIO0.2 |
| DIO0.5 | 6 | 5 | DIO0.4 |
| DIO0.7 | 8 | 7 | DIO0.6 |
| DIO0.9 | 10 | 9 | DIO0.8 |
| DIO0.11 | 12 | 11 | DIO0.10 |
| DIO0.13 | 14 | 13 | DIO0.12 |
| DIO0.15 | 16 | 15 | DIO0.14 |
| GND | 18 | 17 | GND |
| DIO0.17 | 20 | 19 | DIO0.16 |
| DIO0.19 | 22 | 21 | DIO0.18 |
| DIO0.21 | 24 | 23 | DIO0.20 |
| DIO0.23 | 26 | 25 | DIO0.22 |
| DIO0.25 | 28 | 27 | DIO0.24 |
| DIO0.27 | 30 | 29 | DIO0.26 |
| DIO0.29 | 32 | 31 | DIO0.28 |
| DIO0.31 | 34 | 33 | DIO0.30 |
| GND | 36 | 35 | GND |
| +3.3V[1] | 38 | 37 | +3.3V[1] |
| GND | 40 | 39 | GND |

[1] 5V optional. Affects output voltage pin only. Contact RTD Sales for more information

## CN4: Analog I/O Connector

The Analog I/O Connector is a 2 x 25, 0.1" spacing right-angle connector. The pin assignments are shown in the Tables below. A typical mating connector is a FCI 65043-012LF. Pin 1 is indicated by a square solder pad.

| | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin 49 | Pin 47 | Pin 45 | Pin 43 | Pin 41 | Pin 39 | Pin 37 | Pin 35 | Pin 33 | Pin 31 | Pin 29 | Pin 27 | Pin 25 | Pin 23 | Pin 21 | Pin 19 | Pin 17 | Pin 15 | Pin 13 | Pin 11 | Pin 9 | Pin 7 | Pin 5 | Pin 3 | **Pin 1** |
| Pin 50 | Pin 48 | Pin 46 | Pin 44 | Pin 42 | Pin 40 | Pin 38 | Pin 36 | Pin 34 | Pin 32 | Pin 30 | Pin 28 | Pin 26 | Pin 24 | Pin 22 | Pin 20 | Pin 18 | Pin 16 | Pin 14 | Pin 12 | Pin 10 | Pin 8 | Pin 6 | Pin 4 | Pin 2 |

***Table 6: CN4 Differential Mode Pin-out***

| | | | |
|---|---|---|---|
| ADC0.0- | 2 | 1 | ADC0.0+ |
| GND | 4 | 3 | GND |
| ADC1.0- | 6 | 5 | ADC1.0+ |
| GND | 8 | 7 | GND |
| ADC2.0- | 10 | 9 | ADC2.0+ |
| GND | 12 | 11 | GND |
| ADC3.0- | 14 | 13 | ADC3.0+ |
| GND | 16 | 15 | GND |
| ADC4.0- | 18 | 17 | ADC4.0+ |
| GND | 20 | 19 | GND |
| ADC5.0- | 22 | 21 | ADC5.0+ |
| GND | 24 | 23 | GND |
| ADC6.0- | 26 | 25 | ADC6.0+ |
| GND | 28 | 27 | GND |
| ADC7.0- | 30 | 29 | ADC7.0+ |
| GND | 32 | 31 | GND |
| GND | 34 | 33 | DAC0.0 |
| GND | 36 | 35 | DAC1.0 |
| GND | 38 | 37 | DAC2.0 |
| GND | 40 | 39 | DAC3.0 |
| GND | 42 | 41 | DAC4.0 |
| GND | 44 | 43 | DAC5.0 |
| GND | 46 | 45 | DAC6.0 |
| GND | 48 | 47 | DAC7.0 |
| GND | 50 | 49 | +5V[ii] |

***Table 7: CN4 Single-Ended Mode Pin-out***

| | | | |
|---|---|---|---|
| No Connect | 2 | 1 | ADC0.0 |
| GND | 4 | 3 | GND |
| No Connect | 6 | 5 | ADC1.0 |
| GND | 8 | 7 | GND |
| No Connect | 10 | 9 | ADC2.0 |
| GND | 12 | 11 | GND |
| No Connect | 14 | 13 | ADC3.0 |
| GND | 16 | 15 | GND |
| No Connect | 18 | 17 | ADC4.0 |
| GND | 20 | 19 | GND |
| No Connect | 22 | 21 | ADC5.0 |
| GND | 24 | 23 | GND |
| No Connect | 26 | 25 | ADC6.0 |
| GND | 28 | 27 | GND |
| No Connect | 30 | 29 | ADC7.0 |
| GND | 32 | 31 | GND |
| GND | 34 | 33 | DAC0.0 |
| GND | 36 | 35 | DAC1.0 |
| GND | 38 | 37 | DAC2.0 |
| GND | 40 | 39 | DAC3.0 |
| GND | 42 | 41 | DAC4.0 |
| GND | 44 | 43 | DAC5.0 |
| GND | 46 | 45 | DAC6.0 |
| GND | 48 | 47 | DAC7.0 |
| GND | 50 | 49 | +5V[ii] |

[ii] Analog voltage rail can supply up to 1A. Customer must ensure that the current limit is not exceeded.

## CN5: SyncBus Connector

The SyncBus Connector is a 2 x 8, 0.1" spacing right-angle connector. The pin assignments are shown in Table 8 below. A typical mating connector is a FCI 65043-029LF. Pin 1 is indicated by a square solder pad.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin 15 | Pin 13 | Pin 11 | Pin 9 | Pin 7 | Pin 5 | Pin 3 | **Pin 1** |
| Pin 16 | Pin 14 | Pin 12 | Pin 10 | Pin 8 | Pin 6 | Pin 4 | Pin 2 |

***Table 8: CN5 Pin-out***

| | | | |
|---|---|---|---|
| SYNC0- | 2 | 1 | SYNC0+ |
| GND | 4 | 3 | GND |
| SYNC1- | 6 | 5 | SYNC1+ |
| GND | 8 | 7 | GND |
| SYNC2-- | 10 | 9 | SYNC2+ |
| GND | 12 | 11 | GND |
| SYNC3- | 14 | 13 | SYNC3+ |
| GND | 16 | 15 | GND |

## Other Connectors

CN6 is for Factory Use only

### 3.3.3 DM35218 External I/O Connectors

#### CN3: Digital I/O Connector

The Digital I/O Connector is a 2 x 20, 0.1" spacing right-angle connector. The pin assignments are shown in Table 5 below. A typical mating connector is a FCI 65043-017LF. Pin 1 is indicated by a square solder pad.

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin 39 | Pin 37 | Pin 35 | Pin 33 | Pin 31 | Pin 29 | Pin 27 | Pin 25 | Pin 23 | Pin 21 | Pin 19 | Pin 17 | Pin 15 | Pin 13 | Pin 11 | Pin 9 | Pin 7 | Pin 5 | Pin 3 | **Pin 1** |
| Pin 40 | Pin 38 | Pin 36 | Pin 34 | Pin 32 | Pin 30 | Pin 28 | Pin 26 | Pin 24 | Pin 22 | Pin 20 | Pin 18 | Pin 16 | Pin 14 | Pin 12 | Pin 10 | Pin 8 | Pin 6 | Pin 4 | Pin 2 |

***Table 9: CN3 Single-Ended Mode Pin-out***

| | | | |
|---|---|---|---|
| DIO0.1 | 2 | 1 | DIO0.0 |
| DIO0.3 | 4 | 3 | DIO0.2 |
| DIO0.5 | 6 | 5 | DIO0.4 |
| DIO0.7 | 8 | 7 | DIO0.6 |
| DIO0.9 | 10 | 9 | DIO0.8 |
| DIO0.11 | 12 | 11 | DIO0.10 |
| DIO0.13 | 14 | 13 | DIO0.12 |
| DIO0.15 | 16 | 15 | DIO0.14 |
| GND | 18 | 17 | GND |
| DIO0.17 | 20 | 19 | DIO0.16 |
| DIO0.19 | 22 | 21 | DIO0.18 |
| DIO0.21 | 24 | 23 | DIO0.20 |
| DIO0.23 | 26 | 25 | DIO0.22 |
| DIO0.25 | 28 | 27 | DIO0.24 |
| DIO0.27 | 30 | 29 | DIO0.26 |
| DIO0.29 | 32 | 31 | DIO0.28 |
| DIO0.31 | 34 | 33 | DIO0.30 |
| GND | 36 | 35 | GND |
| +3.3V[1] | 38 | 37 | +3.3V[6] |
| GND | 40 | 39 | GND |

[1] 5V optional. Affects output voltage pin only. Contact RTD Sales for more information

## CN4: Analog I/O Connector

The Analog I/O Connector is a 2 x 25, 0.1" spacing right-angle connector. The pin assignments are shown in the Tables below. A typical mating connector is a FCI 65043-012LF. Pin 1 is indicated by a square solder pad.

| | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin 49 | Pin 47 | Pin 45 | Pin 43 | Pin 41 | Pin 39 | Pin 37 | Pin 35 | Pin 33 | Pin 31 | Pin 29 | Pin 27 | Pin 25 | Pin 23 | Pin 21 | Pin 19 | Pin 17 | Pin 15 | Pin 13 | Pin 11 | Pin 9 | Pin 7 | Pin 5 | Pin 3 | **Pin 1** |
| Pin 50 | Pin 48 | Pin 46 | Pin 44 | Pin 42 | Pin 40 | Pin 38 | Pin 36 | Pin 34 | Pin 32 | Pin 30 | Pin 28 | Pin 26 | Pin 24 | Pin 22 | Pin 20 | Pin 18 | Pin 16 | Pin 14 | Pin 12 | Pin 10 | Pin 8 | Pin 6 | Pin 4 | Pin 2 |

***Table 10: CN4 Differential Mode Pin-out***

| | | | |
|---|---|---|---|
| ADC0.0- | 2 | 1 | ADC0.0+ |
| GND | 4 | 3 | GND |
| ADC1.0- | 6 | 5 | ADC1.0+ |
| GND | 8 | 7 | GND |
| ADC2.0- | 10 | 9 | ADC2.0+ |
| GND | 12 | 11 | GND |
| ADC3.0- | 14 | 13 | ADC3.0+ |
| GND | 16 | 15 | GND |
| Reserved | 18 | 17 | Reserved |
| GND | 20 | 19 | GND |
| Reserved | 22 | 21 | Reserved |
| GND | 24 | 23 | GND |
| Reserved | 26 | 25 | Reserved |
| GND | 28 | 27 | GND |
| Reserved | 30 | 29 | Reserved |
| GND | 32 | 31 | GND |
| GND | 34 | 33 | DAC0.0 |
| GND | 36 | 35 | DAC1.0 |
| GND | 38 | 37 | DAC2.0 |
| GND | 40 | 39 | DAC3.0 |
| GND | 42 | 41 | Reserved |
| GND | 44 | 43 | Reserved |
| GND | 46 | 45 | Reserved |
| GND | 48 | 47 | Reserved |
| GND | 50 | 49 | +5V[1] |

***Table 11: CN4 Single-Ended Mode Pin-out***

| | | | |
|---|---|---|---|
| No Connect | 2 | 1 | ADC0.0 |
| GND | 4 | 3 | GND |
| No Connect | 6 | 5 | ADC1.0 |
| GND | 8 | 7 | GND |
| No Connect | 10 | 9 | ADC2.0 |
| GND | 12 | 11 | GND |
| No Connect | 14 | 13 | ADC3.0 |
| GND | 16 | 15 | GND |
| Reserved | 18 | 17 | Reserved |
| GND | 20 | 19 | GND |
| Reserved | 22 | 21 | Reserved |
| GND | 24 | 23 | GND |
| Reserved | 26 | 25 | Reserved |
| GND | 28 | 27 | GND |
| Reserved | 30 | 29 | Reserved |
| GND | 32 | 31 | GND |
| GND | 34 | 33 | DAC0.0 |
| GND | 36 | 35 | DAC1.0 |
| GND | 38 | 37 | DAC2.0 |
| GND | 40 | 39 | DAC3.0 |
| GND | 42 | 41 | Reserved |
| GND | 44 | 43 | Reserved |
| GND | 46 | 45 | Reserved |
| GND | 48 | 47 | Reserved |
| GND | 50 | 49 | +5V[1] |

[1] Analog voltage rail can supply up to 1A. Customer must ensure that the current limit is not exceeded.

## CN5: SyncBus Connector

The SyncBus Connector is a 2 x 8, 0.1" spacing right-angle connector. The pin assignments are shown in Table 8 below. A typical mating connector is a FCI 65043-029LF. Pin 1 is indicated by a square solder pad.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin 15 | Pin 13 | Pin 11 | Pin 9 | Pin 7 | Pin 5 | Pin 3 | **Pin 1** |
| Pin 16 | Pin 14 | Pin 12 | Pin 10 | Pin 8 | Pin 6 | Pin 4 | Pin 2 |

***Table 12: CN5 Pin-out***

| | | | |
|---|---|---|---|
| SYNC0- | 2 | 1 | SYNC0+ |
| GND | 4 | 3 | GND |
| SYNC1- | 6 | 5 | SYNC1+ |
| GND | 8 | 7 | GND |
| SYNC2-- | 10 | 9 | SYNC2+ |
| GND | 12 | 11 | GND |
| SYNC3- | 14 | 13 | SYNC3+ |
| GND | 16 | 15 | GND |

#### Other Connectors

CN6 are for Factory Use only

### 3.3.4 JUMPERS

There are no jumpers on the board.

### 3.3.5 LEDS

#### LED 0: Clock Reset

This LED is used to indicate if the system clock is in reset. When on the system clock is no longer in reset.

#### LED 1: Clock Status

This LED blinks when the systems clock is running.

#### LED 2: SYNCBUS Lock

This LED is on when using the SYNCBUS and the clock is locked.

#### LED 3: Clock Select

This LED is used to indicate which clock is being used. The LED is on when the SYNCBUS is being used as the clock. The LED is off when the onboard oscillator is being used.

## 3.4 Steps for Installing

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the PC/104 system or stack.
3. Select and install stand-offs to properly position the module on the stack.
4. Remove the module from its anti-static bag.
5. Check that pins of the bus connector are properly positioned.
6. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
7. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
8. Gently and evenly press the module onto the PC/104 stack.
9. If any boards are to be stacked above this module, install them.
10. Attach any necessary cables to the PC/104 stack.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

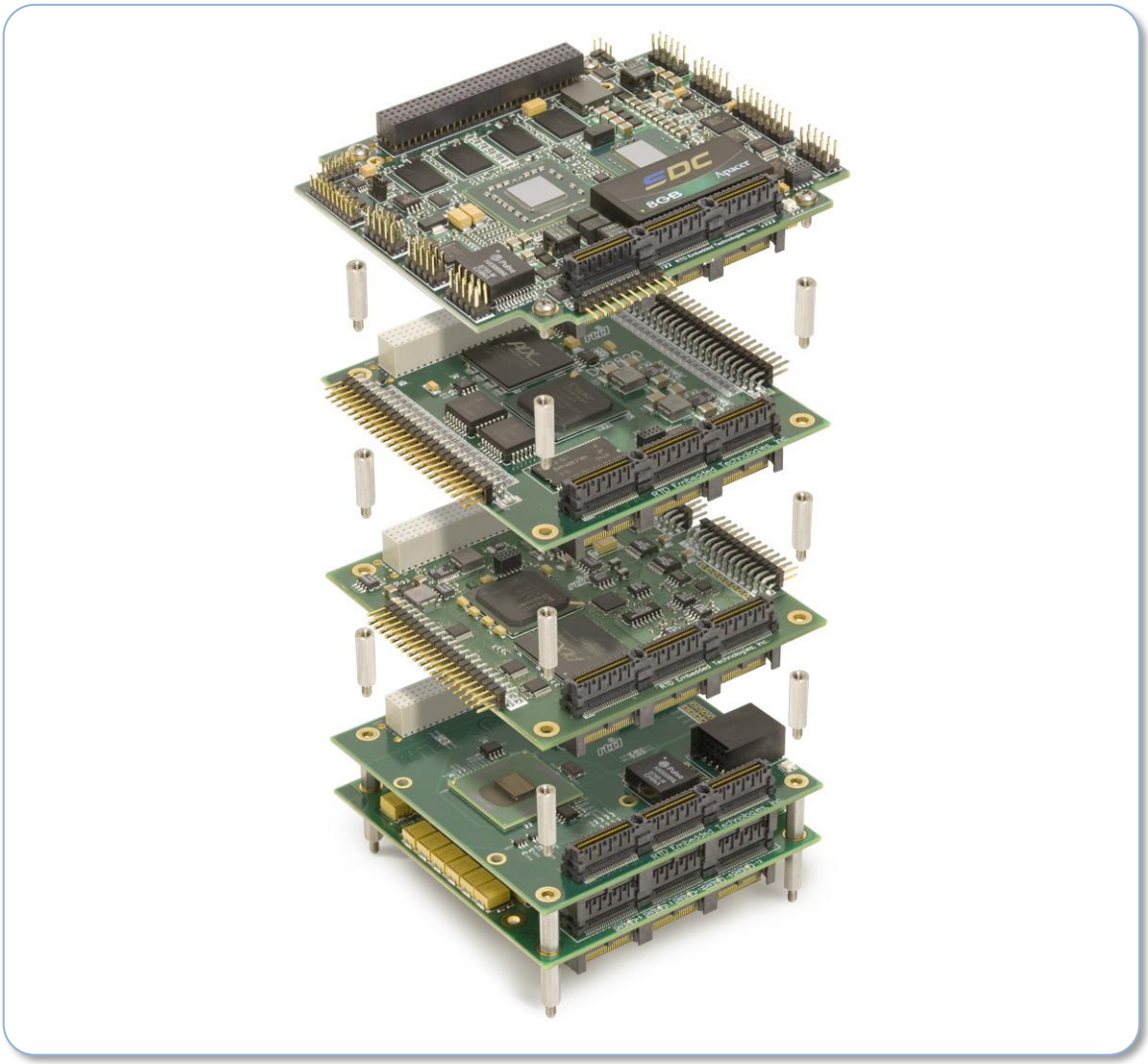


***Figure 5: Example 104™ Stack***

# 4 IDAN Connections

## 4.1 Module Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your module in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the module by the aluminum enclosure, and do not touch the components or connectors. Handle the module in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

## 4.2 Physical Characteristics

- Weight: Approximately 0.21 Kg (0.46 lbs.)
- Dimensions: 152 mm L x 130 mm W x 17 mm H (5.98 in L x 5.12 in W x 0.67 in H)

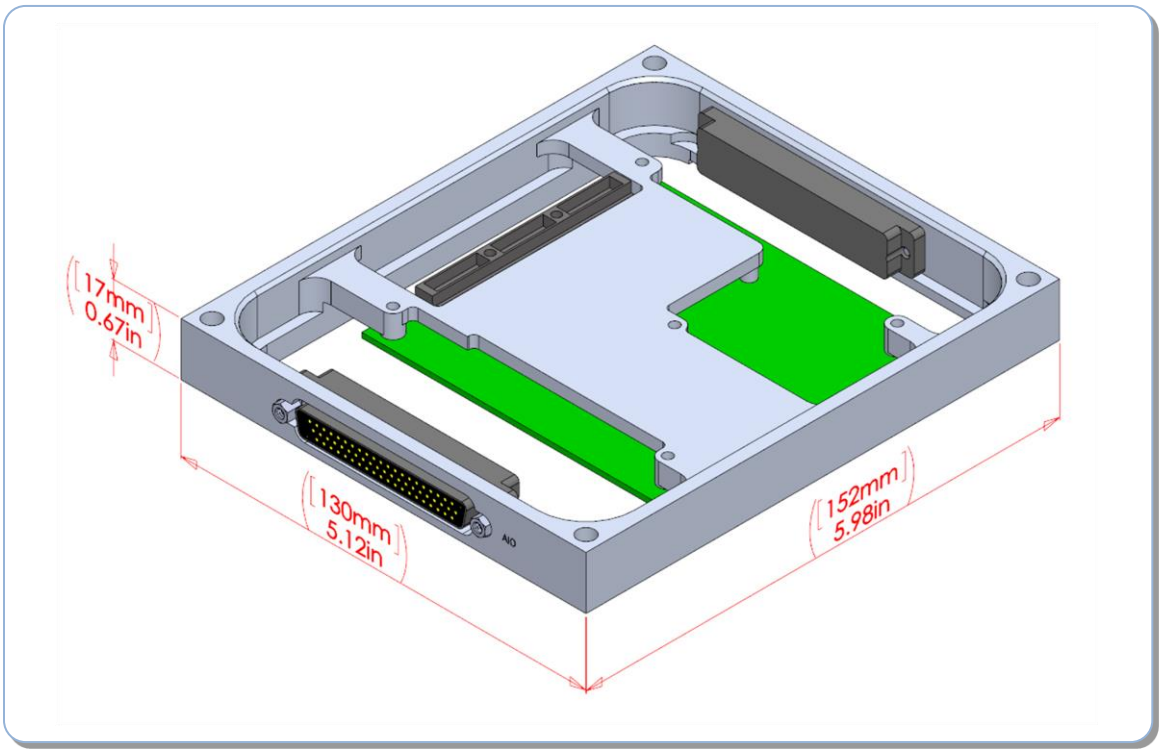
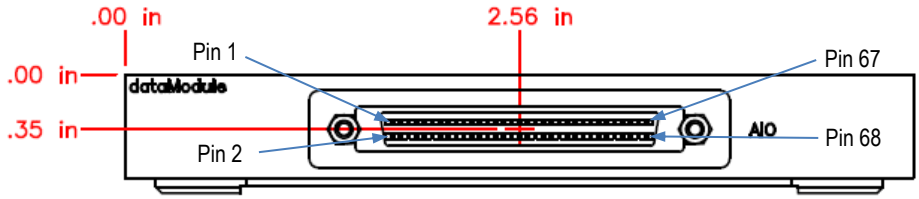



***Figure 6: IDAN Dimensions***

## 4.3 Connectors

### 4.3.1 DM35418 External I/O Connectors

Analog I/O and SyncBus Connector - 68-pin Subminiature "D" Female Connector




**Connector Part #:** Amp 749070-7 **Example Mating Connector:** Amp 786090-7(IDC Crimp)

*Table 13: IDAN- DM35418 68-Pin Subminiature "D" Connector*

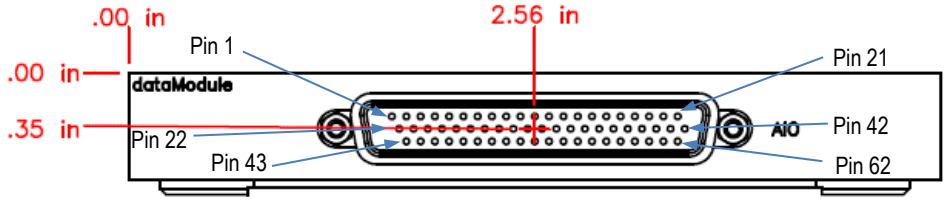
| IDAN Pin# | Signal | DM35418 Pin # | |
|---|---|---|---|
| 1 | ADC0.0+ | CN4 | 1 |
| 2 | ADC0.0- | CN4 | 2 |
| 3 | GND | CN4 | 3 |
| 4 | GND | CN4 | 4 |
| 5 | ADC1.0+ | CN4 | 5 |
| 6 | ADC1.0- | CN4 | 6 |
| 7 | GND | CN4 | 7 |
| 8 | GND | CN4 | 8 |
| 9 | ADC2.0+ | CN4 | 9 |
| 10 | ADC2.0- | CN4 | 10 |
| 11 | GND | CN4 | 11 |
| 12 | GND | CN4 | 12 |
| 13 | ADC3.0+ | CN4 | 13 |
| 14 | ADC3.0- | CN4 | 14 |
| 15 | GND | CN4 | 15 |
| 16 | GND | CN4 | 16 |
| 17 | ADC4.0+ | CN4 | 17 |
| 18 | ADC4.0- | CN4 | 18 |
| 19 | GND | CN4 | 19 |
| 20 | GND | CN4 | 20 |
| 21 | ADC5.0+ | CN4 | 21 |
| 22 | ADC5.0- | CN4 | 22 |
| 23 | GND | CN4 | 23 |
| 24 | GND | CN4 | 24 |
| 25 | ADC6.0+ | CN4 | 25 |
| 26 | ADC6.0- | CN4 | 26 |
| 27 | GND | CN4 | 27 |
| 28 | GND | CN4 | 28 |
| 29 | ADC7.0+ | CN4 | 29 |
| 30 | ADC7.0- | CN4 | 30 |
| 31 | GND | CN4 | 31 |
| 32 | GND | CN4 | 32 |
| 33 | DAC0.0 | CN4 | 33 |
| 34 | GND | CN4 | 34 |

*Table 13: IDAN- DM35418 68-Pin Subminiature "D" Connector*

| IDAN Pin# | Signal | DM35418 Pin # | |
|---|---|---|---|
| 35 | DAC1.0 | CN4 | 35 |
| 36 | GND | CN4 | 36 |
| 37 | DAC2.0 | CN4 | 37 |
| 38 | GND | CN4 | 38 |
| 39 | DAC3.0 | CN4 | 39 |
| 40 | GND | CN4 | 40 |
| 41 | DAC4.0 | CN4 | 41 |
| 42 | GND | CN4 | 42 |
| 43 | DAC5.0 | CN4 | 43 |
| 44 | GND | CN4 | 44 |
| 45 | DAC6.0 | CN4 | 45 |
| 46 | GND | CN4 | 46 |
| 47 | DAC7.0 | CN4 | 47 |
| 48 | GND | CN4 | 48 |
| 49 | +5V Analog[1] | CN4 | 49 |
| 50 | GND | CN4 | 50 |
| 51 | SYNC0+ | CN5 | 1 |
| 52 | SYNC0- | CN5 | 2 |
| 53 | GND | CN5 | 3 |
| 54 | GND | CN5 | 3 |
| 55 | SYNC1+ | CN5 | 5 |
| 56 | SYNC1- | CN5 | 6 |
| 57 | GND | CN5 | 7 |
| 58 | GND | CN5 | 8 |
| 59 | SYNC2+ | CN5 | 9 |
| 60 | SYNC2- | CN5 | 10 |
| 61 | GND | CN5 | 11 |
| 62 | GND | CN5 | 12 |
| 63 | SYNC3+ | CN5 | 13 |
| 64 | SYNC3- | CN5 | 14 |
| 65 | GND | CN5 | 15 |
| 66 | GND | CN5 | 16 |
| 67 | N/C | | |
| 68 | N/C | | |

[1] Analog voltage rail can supply up to 1A. Customer must ensure that the current limit is not exceeded.

## Analog I/O and SyncBus Connector - 62-pin High Density "D" Female Connector




**Connector Part #:** VALCONN HDB-62S

**Example Mating Connector:** VALCONN HDB-62P

*-Table 14: IDAN- DM35418 62-Pin High Density "D" Connector*

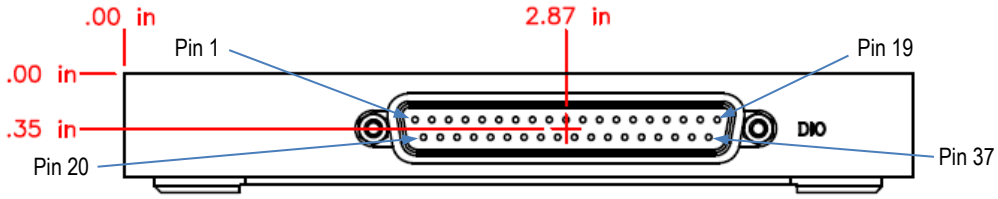
| IDAN Pin# | Signal | DM35418 Pin # | |
|---|---|---|---|
| 1 | ADC0.0+ | CN4 | 1 |
| 2 | GND | CN4 | 4 |
| 3 | GND | CN4 | 7 |
| 4 | ADC2.0- | CN4 | 10 |
| 5 | ADC3.0+ | CN4 | 13 |
| 6 | GND | CN4 | 16 |
| 7 | GND | CN4 | 19 |
| 8 | ADC5.0- | CN4 | 22 |
| 9 | ADC6.0+ | CN4 | 25 |
| 10 | GND | CN4 | 28 |
| 11 | GND | CN4 | 31 |
| 12 | GND | CN4 | 34 |
| 13 | DAC2.0 | CN4 | 37 |
| 14 | GND | CN4 | 40 |
| 15 | DAC5.0 | CN4 | 43 |
| 16 | GND | CN4 | 46 |
| 17 | +5V Analog[1] | CN4 | 49 |
| 18 | GND | CN5 | 12 |
| 19 | SYNC1+ | CN5 | 5 |
| 20 | GND | CN5 | 4 |
| 21 | SYNC0+ | CN5 | 1 |
| 22 | ADC0.0- | CN4 | 2 |
| 23 | ADC1.0+ | CN4 | 5 |
| 24 | GND | CN4 | 8 |
| 25 | GND | CN4 | 11 |
| 26 | ADC3.0- | CN4 | 14 |
| 27 | ADC4.0+ | CN4 | 17 |
| 28 | GND | CN4 | 20 |
| 29 | GND | CN4 | 23 |
| 30 | ADC6.0- | CN4 | 26 |
| 31 | ADC7.0+ | CN4 | 29 |

*-Table 14: IDAN- DM35418 62-Pin High Density "D" Connector*

| IDAN Pin# | Signal | DM35418 Pin # | |
|---|---|---|---|
| 32 | GND | CN4 | 32 |
| 33 | DAC1.0 | CN4 | 35 |
| 34 | GND | CN4 | 38 |
| 35 | DAC4.0 | CN4 | 41 |
| 36 | GND | CN4 | 44 |
| 37 | DAC7.0 | CN4 | 47 |
| 38 | GND | CN4 | 50 |
| 39 | SYNC3- | CN5 | 14 |
| 40 | SYNC1- | CN5 | 6 |
| 41 | SYNC2- | CN5 | 10 |
| 42 | SYNC0- | CN5 | 2 |
| 43 | GND | CN4 | 3 |
| 44 | ADC1.0- | CN4 | 6 |
| 45 | ADC2.0+ | CN4 | 9 |
| 46 | GND | CN4 | 12 |
| 47 | GND | CN4 | 15 |
| 48 | ADC4.0- | CN4 | 18 |
| 49 | ADC5.0+ | CN4 | 21 |
| 50 | GND | CN4 | 24 |
| 51 | GND | CN4 | 27 |
| 52 | ADC7.0- | CN4 | 30 |
| 53 | DAC0.0 | CN4 | 33 |
| 54 | GND | CN4 | 36 |
| 55 | DAC3.0 | CN4 | 39 |
| 56 | GND | CN4 | 42 |
| 57 | DAC6.0 | CN4 | 45 |
| 58 | GND | CN4 | 48 |
| 59 | SYNC3+ | CN5 | 13 |
| 60 | GND | CN5 | 15 |
| 61 | SYNC2+ | CN5 | 9 |
| 62 | GND | CN5 | 7 |

[1] Analog voltage rail can supply up to 1A. Customer must ensure that the current limit is not exceeded.

## Digital I/O Connector - 37-pin High Density "D" Female Connector



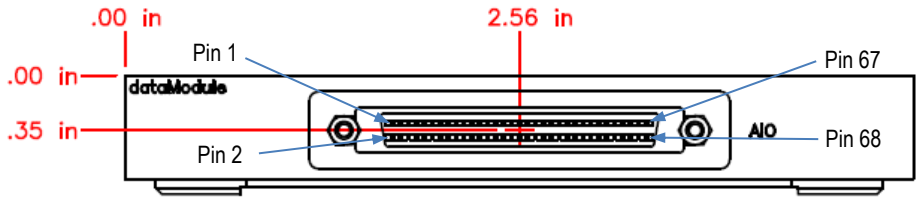

**Connector Part #:** AMP 1658610-1 **Example Mating Connector:** TYCO 1658608-1

*Table 15: IDAN- DM35418 37-Pin High Density "D" Connector*

| IDAN Pin# | Signal | DM35418 Pin # | |
|---|---|---|---|
| 1 | DIO0.0 | CN4 | 1 |
| 2 | DIO0.2 | CN4 | 3 |
| 3 | DIO0.4 | CN4 | 5 |
| 4 | DIO0.6 | CN4 | 7 |
| 5 | DIO0.8 | CN4 | 9 |
| 6 | DIO0.10 | CN4 | 11 |
| 7 | DIO0.12 | CN4 | 13 |
| 8 | DIO0.14 | CN4 | 15 |
| 9 | GND | CN4 | 17 |
| 10 | DIO0.16 | CN4 | 19 |
| 11 | DIO0.18 | CN4 | 21 |
| 12 | DIO0.20 | CN4 | 23 |
| 13 | DIO0.22 | CN4 | 25 |
| 14 | DIO0.24 | CN4 | 27 |
| 15 | DIO0.26 | CN4 | 29 |
| 16 | DIO0.28 | CN4 | 31 |
| 17 | DIO0.30 | CN4 | 33 |
| 18 | GND | CN4 | 35 |
| 19 | +3.3V | CN4 | 37 |
| 20 | DIO0.1 | CN4 | 2 |
| 21 | DIO0.3 | CN4 | 4 |
| 22 | DIO0.5 | CN4 | 6 |
| 23 | DIO0.7 | CN4 | 8 |
| 24 | DIO0.9 | CN4 | 10 |
| 25 | DIO0.11 | CN4 | 12 |
| 26 | DIO0.13 | CN4 | 14 |
| 27 | DIO0.15 | CN4 | 16 |
| 28 | GND | CN4 | 18 |
| 29 | DIO0.17 | CN4 | 20 |
| 30 | DIO0.19 | CN4 | 22 |
| 31 | DIO0.21 | CN4 | 24 |
| 32 | DIO0.23 | CN4 | 26 |
| 33 | DIO0.25 | CN4 | 28 |
| 34 | DIO0.27 | CN4 | 30 |
| 35 | DIO0.29 | CN4 | 32 |
| 36 | DIO0.31 | CN4 | 34 |
| 37 | GND | CN4 | 36 |

### 4.3.2 DM35218 External I/O Connectors

Analog I/O and SyncBus Connector - 68-pin Subminiature "D" Female Connector




**Connector Part #:** Amp 749070-7 **Example Mating Connector:** Amp 786090-7(IDC Crimp)

*Table 16: IDAN- DM35218 68-Pin Subminiature "D" Connector*

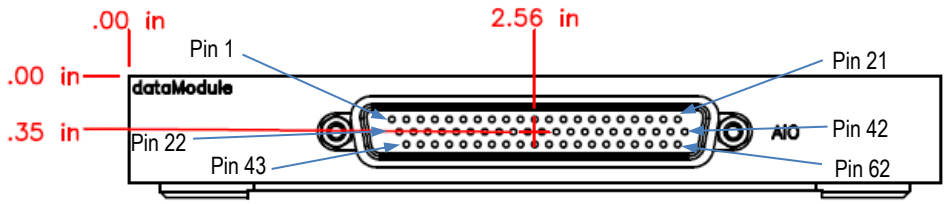
| IDAN Pin# | Signal | DM35218 Pin # | |
|---|---|---|---|
| 1 | ADC0.0+ | CN4 | 1 |
| 2 | ADC0.0- | CN4 | 2 |
| 3 | GND | CN4 | 3 |
| 4 | GND | CN4 | 4 |
| 5 | ADC1.0+ | CN4 | 5 |
| 6 | ADC1.0- | CN4 | 6 |
| 7 | GND | CN4 | 7 |
| 8 | GND | CN4 | 8 |
| 9 | ADC2.0+ | CN4 | 9 |
| 10 | ADC2.0- | CN4 | 10 |
| 11 | GND | CN4 | 11 |
| 12 | GND | CN4 | 12 |
| 13 | ADC3.0+ | CN4 | 13 |
| 14 | ADC3.0- | CN4 | 14 |
| 15 | GND | CN4 | 15 |
| 16 | GND | CN4 | 16 |
| 17 | Reserved | CN4 | 17 |
| 18 | Reserved | CN4 | 18 |
| 19 | GND | CN4 | 19 |
| 20 | GND | CN4 | 20 |
| 21 | Reserved | CN4 | 21 |
| 22 | Reserved | CN4 | 22 |
| 23 | GND | CN4 | 23 |
| 24 | GND | CN4 | 24 |
| 25 | Reserved | CN4 | 25 |
| 26 | Reserved | CN4 | 26 |
| 27 | GND | CN4 | 27 |
| 28 | GND | CN4 | 28 |
| 29 | Reserved | CN4 | 29 |
| 30 | Reserved | CN4 | 30 |
| 31 | GND | CN4 | 31 |
| 32 | GND | CN4 | 32 |
| 33 | DAC0.0 | CN4 | 33 |
| 34 | GND | CN4 | 34 |

*Table 16: IDAN- DM35218 68-Pin Subminiature "D" Connector*

| IDAN Pin# | Signal | DM35218 Pin # | |
|---|---|---|---|
| 35 | DAC1.0 | CN4 | 35 |
| 36 | GND | CN4 | 36 |
| 37 | DAC2.0 | CN4 | 37 |
| 38 | GND | CN4 | 38 |
| 39 | DAC3.0 | CN4 | 39 |
| 40 | GND | CN4 | 40 |
| 41 | Reserved | CN4 | 41 |
| 42 | GND | CN4 | 42 |
| 43 | Reserved | CN4 | 43 |
| 44 | GND | CN4 | 44 |
| 45 | Reserved | CN4 | 45 |
| 46 | GND | CN4 | 46 |
| 47 | Reserved | CN4 | 47 |
| 48 | GND | CN4 | 48 |
| 49 | +5V Analog[1] | CN4 | 49 |
| 50 | GND | CN4 | 50 |
| 51 | SYNC0+ | CN5 | 1 |
| 52 | SYNC0- | CN5 | 2 |
| 53 | GND | CN5 | 3 |
| 54 | GND | CN5 | 4 |
| 55 | SYNC1+ | CN5 | 5 |
| 56 | SYNC1- | CN5 | 6 |
| 57 | GND | CN5 | 7 |
| 58 | GND | CN5 | 8 |
| 59 | SYNC2+ | CN5 | 9 |
| 60 | SYNC2- | CN5 | 10 |
| 61 | GND | CN5 | 11 |
| 62 | GND | CN5 | 12 |
| 63 | SYNC3+ | CN5 | 13 |
| 64 | SYNC3- | CN5 | 14 |
| 65 | GND | CN5 | 15 |
| 66 | GND | CN5 | 16 |
| 67 | N/C | | |
| 68 | N/C | | |

[1] Analog voltage rail can supply up to 1A. Customer must ensure that the current limit is not exceeded.

Analog I/O and SyncBus Connector - 62-pin High Density "D" Female Connector




**Connector Part #:** VALCONN HDB-62S

**Example Mating Connector:** VALCONN HDB-62P

*Table 17: IDAN- DM35218 62-Pin High Density "D" Connector*

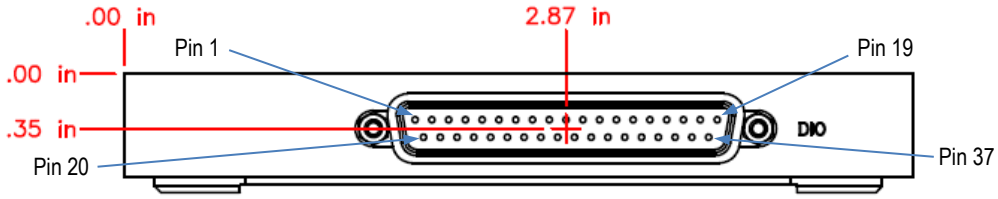
| IDAN Pin# | Signal | DM35218 Pin # | |
|---|---|---|---|
| 1 | ADC0.0+ | CN4 | 1 |
| 2 | GND | CN4 | 4 |
| 3 | GND | CN4 | 7 |
| 4 | ADC2.0- | CN4 | 10 |
| 5 | ADC3.0+ | CN4 | 13 |
| 6 | GND | CN4 | 16 |
| 7 | GND | CN4 | 19 |
| 8 | Reserved | CN4 | 22 |
| 9 | Reserved | CN4 | 25 |
| 10 | GND | CN4 | 28 |
| 11 | GND | CN4 | 31 |
| 12 | GND | CN4 | 34 |
| 13 | DAC2.0 | CN4 | 37 |
| 14 | GND | CN4 | 40 |
| 15 | Reserved | CN4 | 43 |
| 16 | GND | CN4 | 46 |
| 17 | +5V Analog[1] | CN4 | 49 |
| 18 | GND | CN5 | 12 |
| 19 | SYNC1+ | CN5 | 5 |
| 20 | GND | CN5 | 4 |
| 21 | SYNC0+ | CN5 | 1 |
| 22 | ADC0.0- | CN4 | 2 |
| 23 | ADC1.0+ | CN4 | 5 |
| 24 | GND | CN4 | 8 |
| 25 | GND | CN4 | 11 |
| 26 | ADC3.0- | CN4 | 14 |
| 27 | Reserved | CN4 | 17 |
| 28 | GND | CN4 | 20 |
| 29 | GND | CN4 | 23 |
| 30 | Reserved | CN4 | 26 |
| 31 | Reserved | CN4 | 29 |

*Table 17: IDAN- DM35218 62-Pin High Density "D" Connector*

| IDAN Pin# | Signal | DM35418 Pin # | |
|---|---|---|---|
| 32 | GND | CN4 | 32 |
| 33 | DAC1.0 | CN4 | 35 |
| 34 | GND | CN4 | 38 |
| 35 | Reserved | CN4 | 41 |
| 36 | GND | CN4 | 44 |
| 37 | Reserved | CN4 | 47 |
| 38 | GND | CN4 | 50 |
| 39 | SYNC3- | CN5 | 14 |
| 40 | SYNC1- | CN5 | 6 |
| 41 | SYNC2- | CN5 | 10 |
| 42 | SYNC0- | CN5 | 2 |
| 43 | GND | CN4 | 3 |
| 44 | ADC1.0- | CN4 | 6 |
| 45 | ADC2.0+ | CN4 | 9 |
| 46 | GND | CN4 | 12 |
| 47 | GND | CN4 | 15 |
| 48 | Reserved | CN4 | 18 |
| 49 | Reserved | CN4 | 21 |
| 50 | GND | CN4 | 24 |
| 51 | GND | CN4 | 27 |
| 52 | Reserved | CN4 | 30 |
| 53 | DAC0.0 | CN4 | 33 |
| 54 | GND | CN4 | 36 |
| 55 | DAC3.0 | CN4 | 39 |
| 56 | GND | CN4 | 42 |
| 57 | Reserved | CN4 | 45 |
| 58 | GND | CN4 | 48 |
| 59 | SYNC3+ | CN5 | 13 |
| 60 | GND | CN5 | 15 |
| 61 | SYNC2+ | CN5 | 9 |
| 62 | GND | CN5 | 7 |

[1]Analog voltage rail can supply up to 1A. Customer must ensure that the current limit is not exceeded.

## Digital I/O Connector - 37-pin High Density “D” Female Connector




**Connector Part #:** AMP 1658610-1 **Example Mating Connector:** TYCO 1658608-1

***Table 18: IDAN- DM35218 37-Pin High Density "D" Connector***

| IDAN Pin# | Signal | DM35218 Pin # | |
|---|---|---|---|
| 1 | DIO0.0 | CN4 | 1 |
| 2 | DIO0.2 | CN4 | 3 |
| 3 | DIO0.4 | CN4 | 5 |
| 4 | DIO0.6 | CN4 | 7 |
| 5 | DIO0.8 | CN4 | 9 |
| 6 | DIO0.10 | CN4 | 11 |
| 7 | DIO0.12 | CN4 | 13 |
| 8 | DIO0.14 | CN4 | 15 |
| 9 | GND | CN4 | 17 |
| 10 | DIO0.16 | CN4 | 19 |
| 11 | DIO0.18 | CN4 | 21 |
| 12 | DIO0.20 | CN4 | 23 |
| 13 | DIO0.22 | CN4 | 25 |
| 14 | DIO0.24 | CN4 | 27 |
| 15 | DIO0.26 | CN4 | 29 |
| 16 | DIO0.28 | CN4 | 31 |
| 17 | DIO0.30 | CN4 | 33 |
| 18 | GND | CN4 | 35 |
| 19 | +3.3V | CN4 | 37 |
| 20 | DIO0.1 | CN4 | 2 |
| 21 | DIO0.3 | CN4 | 4 |
| 22 | DIO0.5 | CN4 | 6 |
| 23 | DIO0.7 | CN4 | 8 |
| 24 | DIO0.9 | CN4 | 10 |
| 25 | DIO0.11 | CN4 | 12 |
| 26 | DIO0.13 | CN4 | 14 |
| 27 | DIO0.15 | CN4 | 16 |
| 28 | GND | CN4 | 18 |
| 29 | DIO0.17 | CN4 | 20 |
| 30 | DIO0.19 | CN4 | 22 |
| 31 | DIO0.21 | CN4 | 24 |
| 32 | DIO0.23 | CN4 | 26 |
| 33 | DIO0.25 | CN4 | 28 |
| 34 | DIO0.27 | CN4 | 30 |
| 35 | DIO0.29 | CN4 | 32 |
| 36 | DIO0.31 | CN4 | 34 |
| 37 | GND | CN4 | 36 |

### 4.3.3 BUS CONNECTORS

#### CN1(Top) & CN2(Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 58)

The DM35418HR/DM35218HR is a "Universal" board, and can connect to either a Type 1 or Type 2 PCIe/104 connector.

## 4.4 Steps for Installing

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the IDAN system.
3. Remove the module from its anti-static bag.
4. Check that pins of the bus connector are properly positioned.
5. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
6. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
7. Gently and evenly press the module onto the IDAN system.
8. If any boards are to be stacked above this module, install them.
9. Finish assembling the IDAN stack by installing screws of an appropriate length.
10. Attach any necessary cables to the IDAN system.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

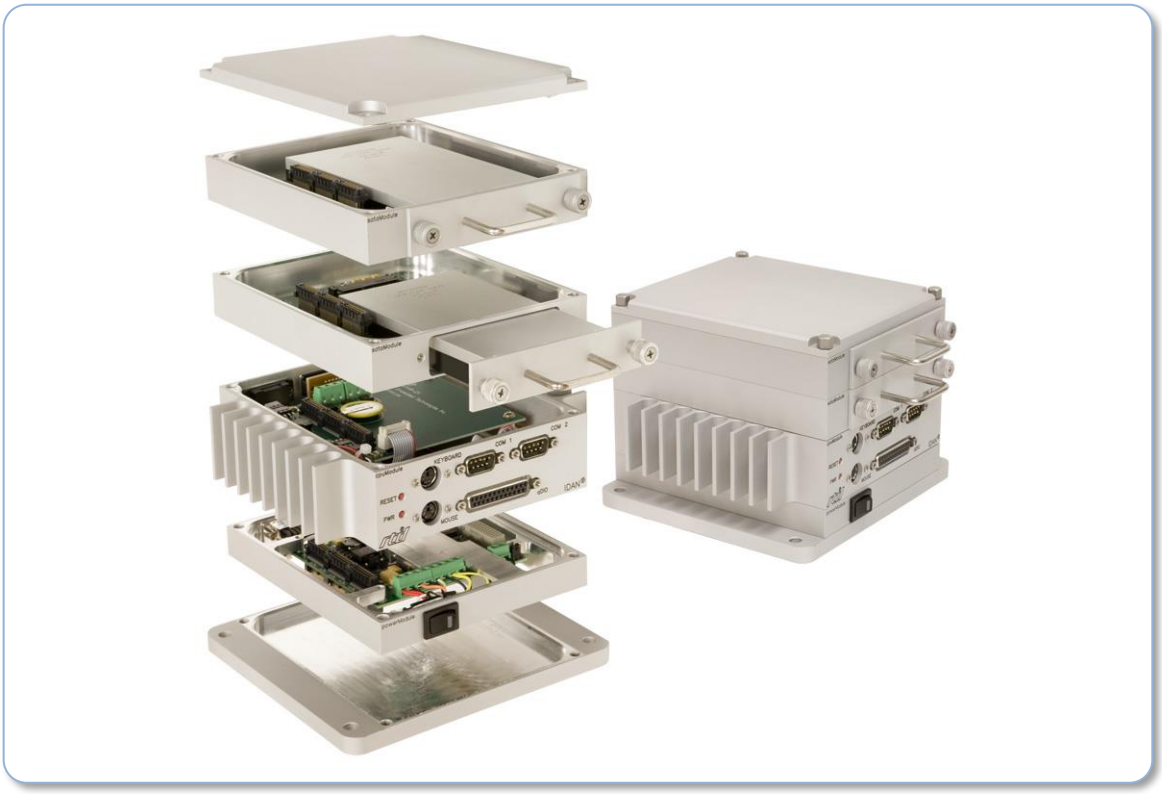


***Figure 7: Example IDAN System***

# 5 Functional Description

## 5.1 Block Diagram

The Figure below shows the functional block diagram of the DM35418HR/DM35218HR. The various parts of the block diagram are discussed in the following sections.

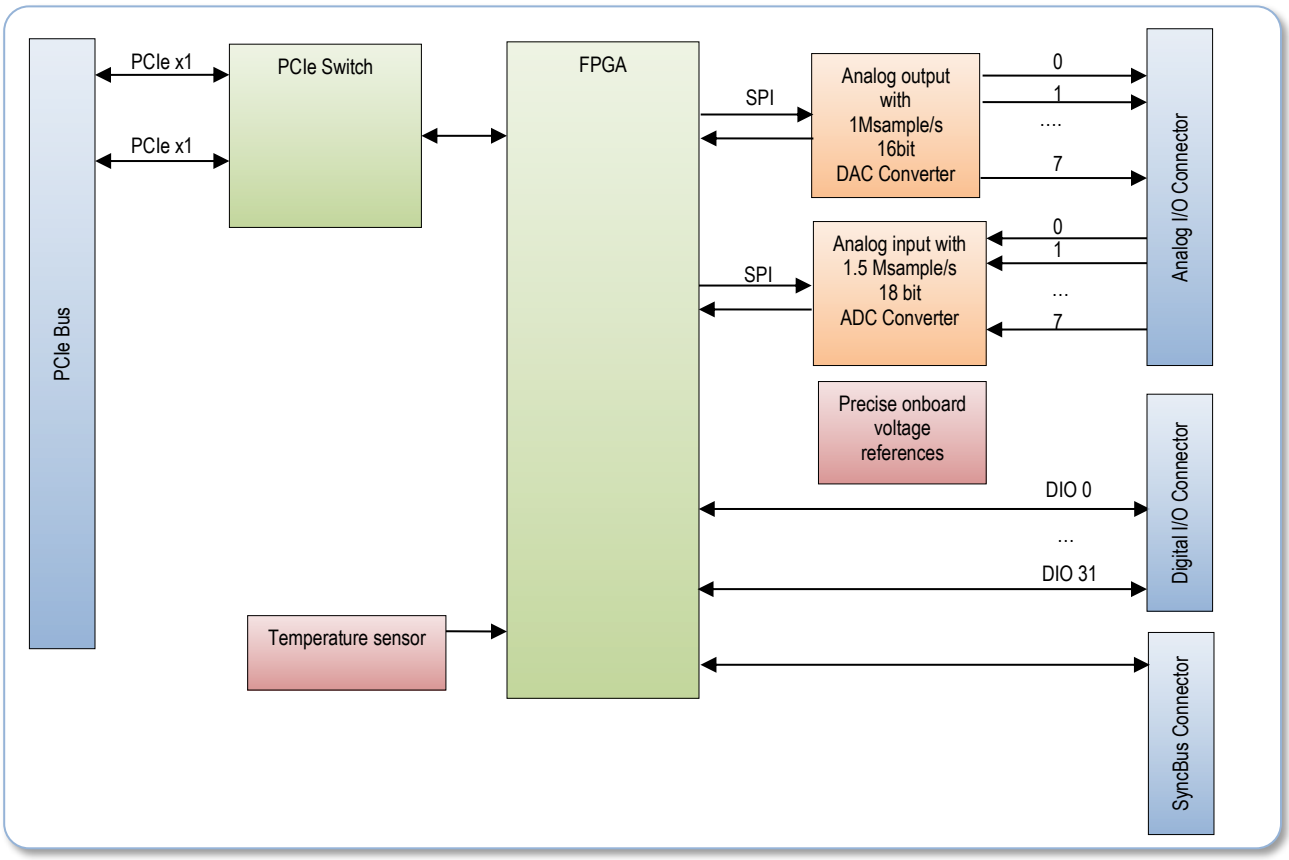



***Figure 8: DM35418HR/DM35218HR Block Diagram***

## 5.2 FPGA with DMA Engine

The DM35418HR/DM35218HR features a FPGA with a built in PCI Express interface and DMA engine. The FPGA controls all communication between the bus and the control logic on the board. The FPGA also features small FIFOs for use with DMA, which is needed for continuous data transfer. Each DAC and ADC is provided with its own FIFO and DMA channel, allowing them to transfer data independent of one another.

Each DMA channel can be programmed to transfer data from FPGA to PCIe bus or from the PCIe bus to the FPGA. Each DMA channel also features a 64-bit PCI addressing and a 16MB maximum buffer for memory accessing.

## 5.3 SyncBus

This module features an LVDS SyncBus. The SyncBus provides the user with three event based triggering lines and one 10MHz based master clock. All four are software configurable for input/output. To use any of the SyncBus lines the module must be configured to use the SyncBus master clock.

SyncBus0 – SyncBus2 lines on CN5 are the user event triggering. When these lines are assigned as output, they can output any of the clocks find in SB_n_CLK_SRC section on page 56. When lines are assigned as an input, they can be assigned as a CLK_BUSn register on page 56, which can be then used to trigger events.

SyncBus3 on CN5 is the master clock. This clock is used to synchronize multiple boards featuring the LVDS SyncBus. To synchronize multiple boards, you must set one board as an output and the rest as inputs. The board that is set as an output, the master will drive a 10MHz clock on

SyncBus3 to synchronize all the boards set as inputs, or slaves. Once boards are synchronized the PLL_LOCKED register will be set to '1' indicating it is now stable and ready to use.

***NOTE: Only enable one output per SyncBus line when synchronizing multiple boards. Enabling multiple outputs on a SyncBus line will result in unexpected behavior.***

## 5.4 Digital I/O

This module provides 32-bits of bi-directional digital I/O. Each bit is programmable as either an input or output. On power cycle, all digital I/O lines are programmed as inputs, meaning that the digital I/O line's initial state is undetermined. If the digital I/O lines must power up to a known state, an external 10 kΩ resistor must be added to pull the line high or low.

Refer to BAR2: Digital I/O (DIO) section on page 53 for more information on register configuration.

## 5.5 Temperature Sensor

This module provides an on board temperature sensor. This sensor provides the module's ambient temperature. Refer to Board Connections figure on page 15 for temperature sensor location.

The temperature sensor provides a signed 12-bit value that capable of measuring temperatures within ±2°C. The temperature sensor is read continuously, approximately every 1 to 2 seconds. This value is then automatically updated in the register. Refer to TEMPERATURE_VAL section on page 54 for more register information.

## 5.6 Analog input

The DM35418HR/DM35218HR has 4/8 independent 18-bit SAR ADC converters, to provide high speed and high digital resolution of the analog input. The ADC converter has a max throughput of 1.5MHz per channel. The high input impedance, low distortion, low noise operation design gives you accurate results. This module also provides ±28V overvoltage input protection to the analog connector (CN4).

The DM35418HR/DM35218HR has a programmable input. This provides the user the ability to select single-ended/differential input, full-scale input range, and unipolar/bipolar input.

Each ADC converter supports a 511 sample FIFO for DMA. Each sample packed into a 32-bit word.

### Single-Ended Input Mode

In single-ended mode, the input signal is measured in reference to the boards GND. In this mode the input signal is connected to input ADC0.0+ through ADC1.0+, and the low side to any of the GND pins available on the Analog Connector.

### Differential Input Mode

In this mode your signal source may or may not have a separate ground reference. In differential mode, the high side input is measured in reference to the low side input. In this mode you connect the high side of the input signal to the analog input, ADC0.0+ through ADC7.0+, and connect the low side to corresponding ADC - pin. When in differential mode, both the high and low side must stay within +/-10V with respect to the board ground. In most cases, the board ground must still be attached to the device that is generating the input signal.

### Full-Scale Input Range

The DM35418HR/DM35218HR has a programmable gain input per channel. This gain can be programed for 1,2,4,8 to achieve input ranges ±5V, ±2.5V, ±1.25V, ±0.625V.

Refer to Table 19 on page 33 for full-scale ranges for both unipolar and bipolar modes.

### Bipolar/Unipolar Mode

In bipolar mode the data is collected in two's complement format. In this format the MSB of the data is the sign bit. If the MSB is "0" the output data is positive value. If the MSB is "1" the output code is negative. The 18-bits of data is sign-extended into a 32-bit word before transferring to the FIFO.

In unipolar mode there is no sign bit, since all values are positive. When the output code is all "0" the input voltage is 0 volts. When the output code is all "1" the input voltage is 10 volts when the gain is set to 1.

Voltage values for each bit will vary depending on input range and gain. For example, if the input is set for ±5, the formula for calculating voltage is as follows:

$$Voltage = \frac{Input\ Range}{2^{18}} \times Conversion\ Data$$

$$Voltage = \frac{10}{2^{18}} \times Conversion\ Data$$

$$Voltage = 38.15\mu V \times Conversion\ Data$$

### 5.6.1 INITIALIZING THE ADC CONVERTER

The following is a list of the typical steps needed to initialize the ADC converter and begin sampling:

1. Set the ADC to the Uninitialized state (MODE = Uninitialized)
2. Setup the DMA for the channel
3. Set the input mode (CH_FRONT_END_CONFIG)
4. Set the start and stop triggers (START_TRIG, STOP_TRIG)
5. Set the clock source (CLK_SOURCE)
6. Set the sample rate (CLK_DIV_CNTR)
7. Set the Pre and/or Post Capture counters (PRE_TRIGGER_CAPTURE, POST_STOP_CAPTURE)
8. Set the ADC to the Reset state (MODE = Reset)
9. Start the DMA
10. Start the ADC (MODE = Go)

### 5.6.2 SIMPLIFIED BLOCK DIAGRAM OF ANALOG INPUT

The following figure shows the front end circuit for the DM35418HR/DM35218HR. It also shows the names of the FPGA registers in bold and the different ways the front-end can be configured for different modes of operation.

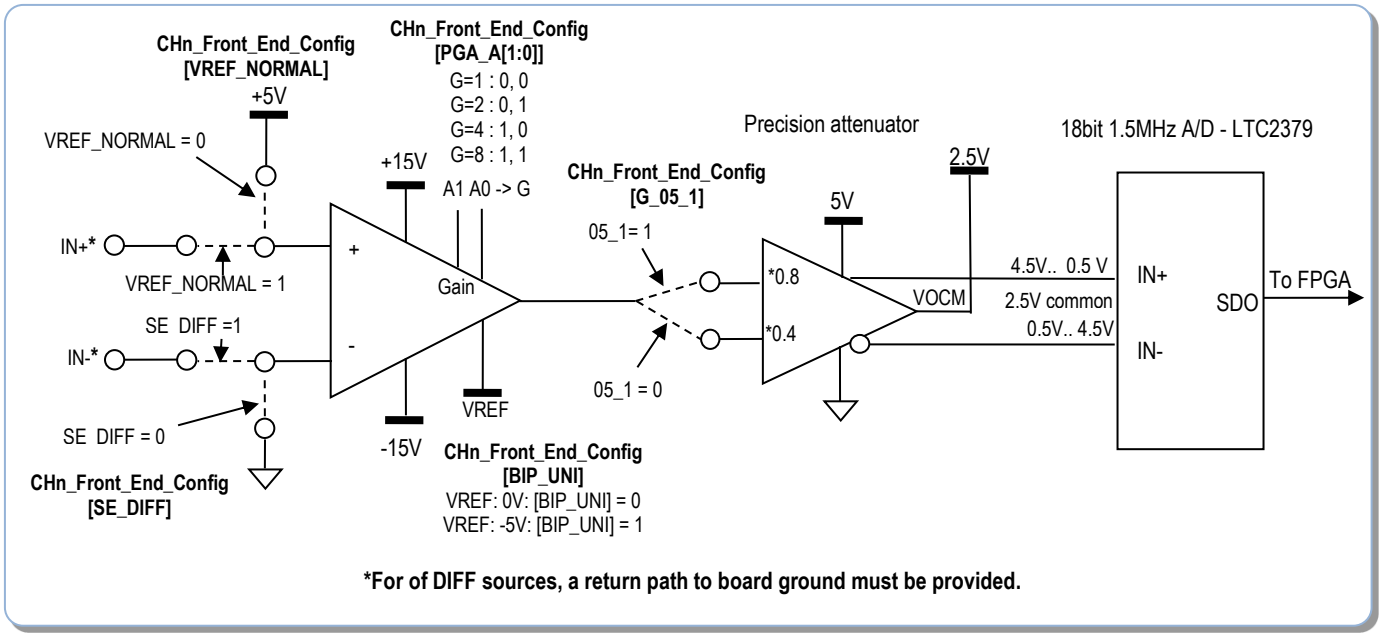



*Figure 9: Analog Input Front End*

*Table 19: ADC Full-Scale Settings*

| CHn_Front_End_Config [PGA_A1] | CHn_Front_End_Config [PGA_A0] | CHn_Front_End_Config [G_05_1] | Signal Path Gain | Unipolar Mode | Bipolar Mode |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0.5 | n/a | ±10V |

*Table 19: ADC Full-Scale Settings*

| CHn_Front_End_Config [PGA_A1] | CHn_Front_End_Config [PGA_A0] | CHn_Front_End_Config [G_05_1] | Signal Path Gain | Unipolar Mode | Bipolar Mode |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0-10V | ±5V |
| 0 | 1 | 1 | 2 | 0-5V | ±2.5V |
| 1 | 0 | 1 | 4 | 0-2.5V | ±1.25V |
| 1 | 1 | 1 | 8 | 0-1.25V | ±0.625V |

Refer to section 6.4.15 for more information about FPGA register control

## 5.6.3 INPUT CONNECTION EXAMPLES

### 5.4.3.1. Single Ended, Bipolar, ±10V Full-scale range

The following figure shows an example how to set up the FPGA registers for a single-ended, bipolar signal with a gain of 1. Also provided are graphs showing the difference between the input vs. output from the PGA.

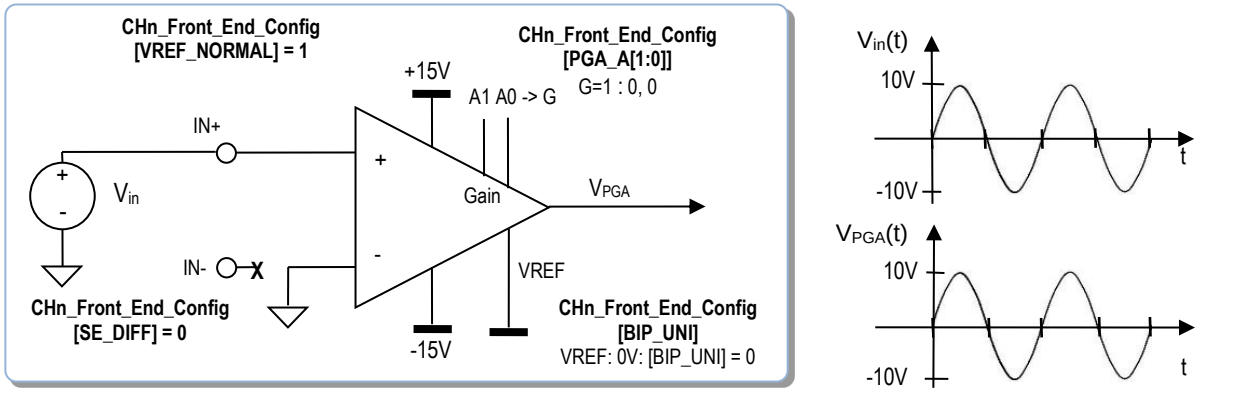



*Figure 10: Bipolar Single-Ended Example*

### 5.4.3.2. Differential, Bipolar, ±10V Full-scale range

The following figure shows an example how to set up the FPGA registers for a differential, bipolar signal with a gain of 1. Also provided are graphs showing the difference between the inputs vs. output from the PGA.

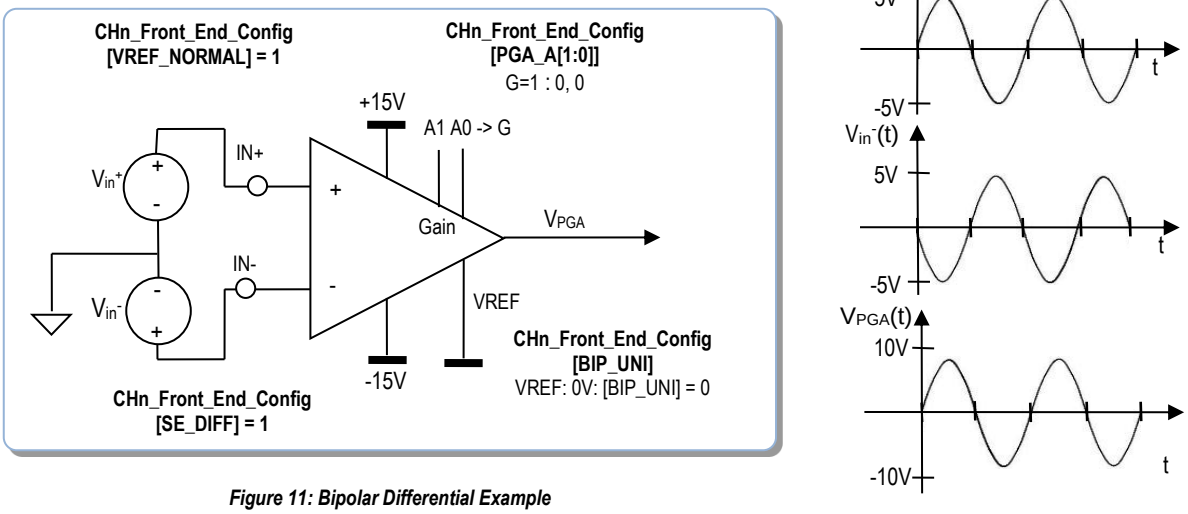



*Figure 11: Bipolar Differential Example*

### 5.4.3.3. Single Ended, Unipolar, 0-10V Full-scale range

The following figure shows an example how to set up the FPGA registers for a single-ended, unipolar signal with a gain of 1. Also provided are graphs showing the difference between the input vs. output from the PGA.

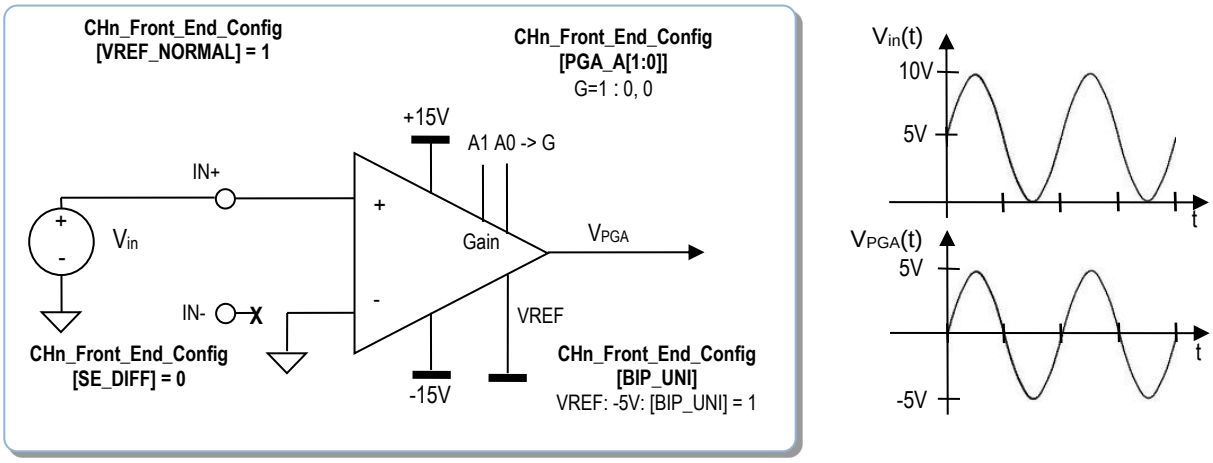



***Figure 12: Unipolar Single Ended Example***

### 5.4.3.4. Differential, Unipolar, 0-10V Full-scale range

The following figure shows an example how to set up the FPGA registers for a differential, unipolar signal with a gain of 1. Also provided are graphs showing the difference between the input vs. output from the PGA.

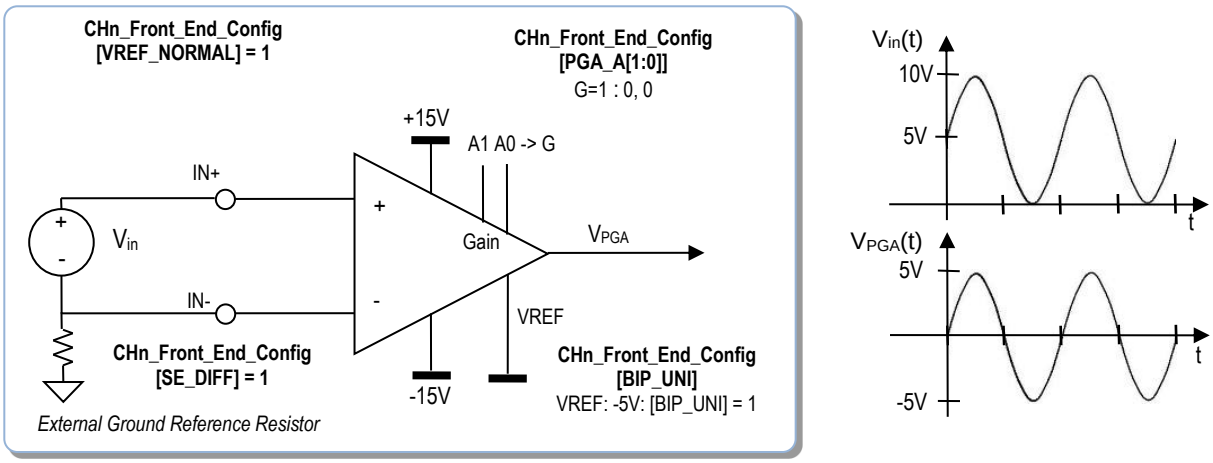



***Figure 13: Unipolar Differential Example***

#### 5.4.3.5. ADC Gain and Offset Test

The following figure shows an example how to set up the FPGA registers to test the offset and gain of each channel. Figure 14 show the front end and FPGA register settings for bipolar operation. Figure 14 show the front end and FPGA register settings for unipolar operation.

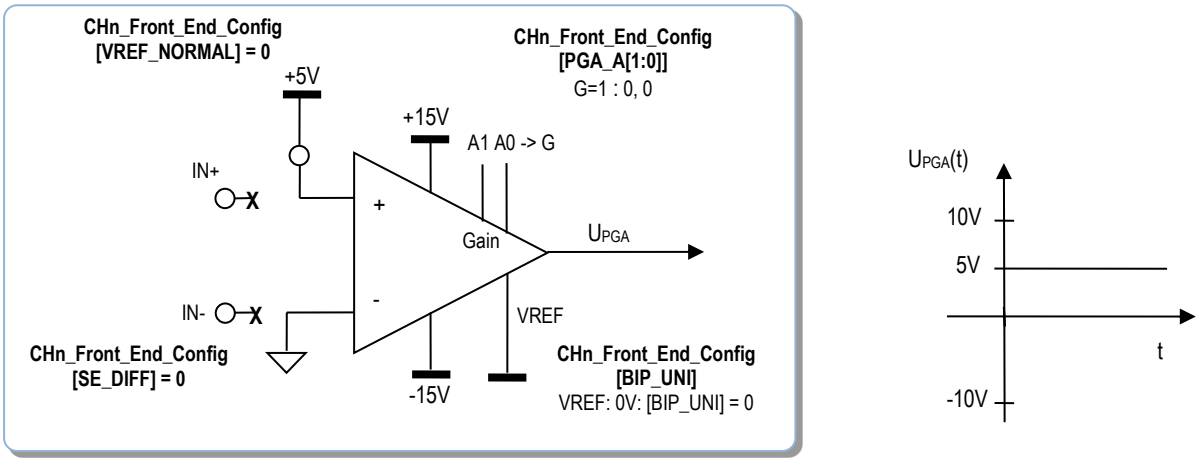



***Figure 14: Bipolar Offset and Gain Test Circuit***

## 5.7 Analog output

The DM35418HR/DM35218HR feature 4/8 independent 16-bit analog output channels with individually programmable output ranges of ±2.5V, ±5V, and ±10V. Each channel supports a maximum update rate 1 MHz and a maximum operating load of 5mA. Each channel has less than 1 Ω of output impedance.

Each DAC converter has a 511 sample FIFO for DMA. Each sample is packed into 32 bits, right justified and sign-extended.

### 5.7.1 Initializing the DAC Converter

The following is a list of the typical steps needed to initialize the DAC converter and begin sampling:

1. Set the DAC to the Uninitialized state (MODE = Uninitialized)
2. Setup the DMA for the channel
3. Set the input mode (CH_FRONT_END_CONFIG)
4. Set the start and stop triggers (START_TRIG, STOP_TRIG)
5. Set the clock source (CLK_SOURCE)
6. Set the sample rate (CLK_DIV_CNTR)
7. Set the Post Capture counter (POST_STOP_CAPTURE)
8. Set the DAC to the Reset state (MODE = Reset)
9. Start the DMA
10. Start the DAC (MODE = Go)

### 5.7.2 SIMPLIFIED BLOCK DIAGRAM OF ANALOG OUTPUT

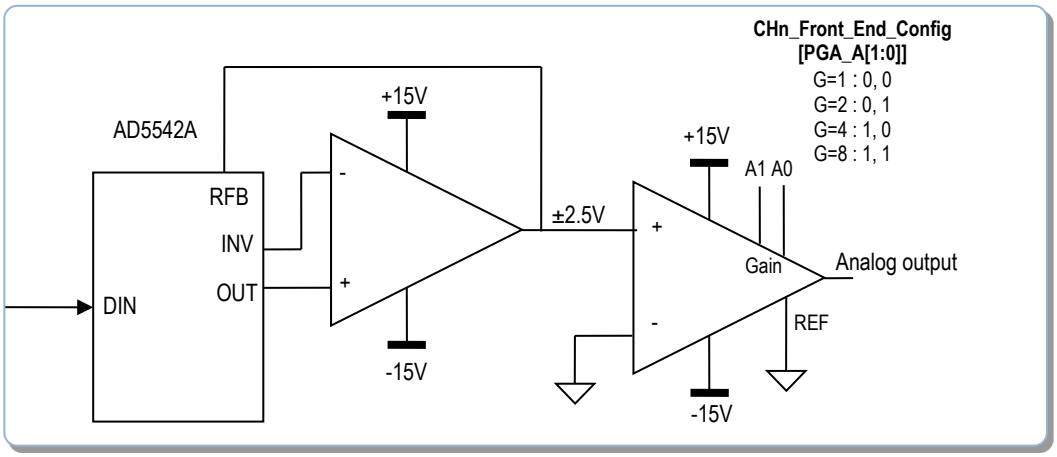



*Figure 15: Analog Output*

*Table 20: DAC Full-Scale Settings*

| CHn_Front_End_Config [PGA_A1] | CHn_Front_End_Config [PGA_A0] | Gain | Bipolar Mode |
|---|---|---|---|
| 0 | 0 | 1 | ±2.5V |
| 0 | 1 | 2 | ±5V |
| 1 | 0 | 4 | ±10V |
| 1 | 1 | 8 | n/a |

*Table 21: Key DAC Bit Weight*

| DAC Bit Weight | Ideal Output Voltages (mV) | | |
|---|---|---|---|
| | -2.5 to +2.5 V | -5 to +5 V | -10 to +10 V |
| 1111 1111 1111 1111 | +2499.9237 | +4999.8474 | +9999.6948 |
| 1000 0000 0000 0001 | 0.0763 | 0.1526 | 0.3052 |
| 1000 0000 0000 0000 | 0.00 | 0.00 | 0.00 |
| 0111 1111 1111 1111 | -0.0763 | +0.1526 | -0.3052 |
| 0000 0000 0000 0000 | -2500.00 | -5000.00 | -10000.00 |

# 6 Register Address Space

This product was built as a modular design, which allows each board function to have its own Functional Block (FB). Each functional block is designed to work independently. For this reason, we provide individual DMA channels, interrupts, clocks, and FIFOs to each functional block.

The registers are described by their PCIe Base Address Register (BAR), which is defined in the PCI configuration space for this board. The configuration space is generally handled by the operating system. For more information on how to use the configuration space, consult the *PCI Local Bus Specification, Revision 3.0* from the PCI-SIG.

## Register Types

There are several different types of registers that are referred to in this section. A description of each type is below.

- Read/Write Registers: The value that is written to this register can also be read back.
- Maskable Registers: This is a 32 bit register that consists of 16-bit data field in the upper word and a 16-bit mask value in the lower word. For each bit in the data field, it is only written to the register if the corresponding bit in the mask field is '1'.
- Sticky Registers: This is a status read register. When a bit in this register has a value of '1', a '1' needs written to that bit to reset the register to '0'. This is typically used for interrupt status registers.
- Read Only: This register can only be read.

***NOTE: Writing to Read-Only registers may have unexpected results.***

## Function Block Mapping

Below is the Function Block slot mapping for the DM35418HR/DM35218HR.

***Table 22: Function Block Mapping***

| Slot | ID | Description | Connector |
|---|---|---|---|
| FB0 | 0x01021000 | Analog to Digital Converter | CN4 ADC0 |
| FB1 | 0x01021000 | Analog to Digital Converter | CN4 ADC1 |
| FB2 | 0x01021000 | Analog to Digital Converter | CN4 ADC2 |
| FB3 | 0x01021000 | Analog to Digital Converter | CN4 ADC3 |
| FB4 | 0x01021000 | Analog to Digital Converter | CN4 ADC4 |
| FB5 | 0x01021000 | Analog to Digital Converter | CN4 ADC5 |
| FB6 | 0x01021000 | Analog to Digital Converter | CN4 ADC6 |
| FB7 | 0x01021000 | Analog to Digital Converter | CN4 ADC7 |
| FB8 | 0x01022000 | Digital to Analog Converter | CN4 DAC0 |
| FB9 | 0x01022000 | Digital to Analog Converter | CN4 DAC1 |
| FB10 | 0x01022000 | Digital to Analog Converter | CN4 DAC2 |
| FB11 | 0x01022000 | Digital to Analog Converter | CN4 DAC3 |
| FB12 | 0x01022000 | Digital to Analog Converter | CN4 DAC4 |
| FB13 | 0x01022000 | Digital to Analog Converter | CN4 DAC5 |
| FB14 | 0x01022000 | Digital to Analog Converter | CN4 DAC6 |
| FB15 | 0x01022000 | Digital to Analog Converter | CN4 DAC7 |
| FB16 | 0x00003000 | Digital I/O | CN3 |
| FB17 | 0x0000F001 | Temperature Sensor | N/A |
| FB18 | 0x00000001 | SyncBus Driver | CN5 |

## 6.1 BAR0: General Board Control

This section contains the board-level interrupt control, as well as a description of all of the Functional Blocks in BAR2. Most of the registers in this section are Read-Only. Although a full implementation requires BAR0 to be 0x400 in length, most implementations will have a shorter length.

*Table 23: Base Functional Block*

| Offset | 0x03 | 0x02 | 0x01 | 0x00 |
|---|---|---|---|---|
| 0x00 | GBC_BRD_RST | GBC_EOI | GBC_REV | GBC_FMT |
| 0x04 | GBC_PDP | | | |
| 0x08 | GBC_BUILD | | | |
| 0x0C | *Reserved* | GBC_USER_ID | GBC_SYS_CLK_FREQ | |
| 0x10 | GBC_IRQ_STATUS | | | |
| 0x14 | | | | |
| 0x18 | GBC_DIRQ_STATUS | | | |
| 0x1C | | | | |
| 0x20 | FB0_ID | | | |
| 0x24 | FB0_OFFSET | | | |
| 0x28 | FB0_OFFSET_DMA | | | |
| 0x2C | reserved | | | |
| 0x30 | FB1_ID | | | |
| 0x34 | FB1_OFFSET | | | |
| 0x38 | FB1_OFFSET_DMA | | | |
| 0x3C | reserved | | | |
| … | | | | |
| 0x20+0x10*n | FBn_ID | | | |
| 0x24+0x10*n | FBn_OFFSET | | | |
| 0x28+0x10*n | FBn_OFFSET_DMA | | | |
| 0x2C+0x10*n | reserved | | | |
| … | | | | |
| 0x3F0 | FB61_ID | | | |
| 0x3F4 | FB61_OFFSET | | | |
| 0x3F8 | FB61_OFFSET_DMA | | | |
| 0x3FC | reserved | | | |

### 6.1.1 GBC_FMT (READ-ONLY)

This register contains the format ID that is used in this board.

- B[7:4] Major Format – Changes to this value indicate changes that are not backward compatible.
  - 0 – Initial Major Format
- B[3:0] Minor Format – Changes to this value indicate additional features that are backward compatible.
  - 1 – Initial Minor Format
  - 2 – Addition of FB_DMAm_CTRLn[Pause] flag and Early DMA Buffer Termination.

### 6.1.2 GBC_REV (READ-ONLY)

This register contains the PDP revision for this board. A=1, B=2, etc.

### 6.1.3 GBC_BRD_RST (READ/WRITE)

Write a value of 0xAA to this register to reset the board.

### 6.1.4 GBC_PDP (READ-ONLY)

This register contains the PDP number for this board in decimal.

### 6.1.5 GBC_BUILD (READ-ONLY)

Unique 32-bit build number for every FPGA build.

### 6.1.6 GBC_SYS_CLK_FREQ (READ ONLY)

The measured frequency of the system clock. Units are 10 kHz, i.e. (Frequency in Hertz) = (GBC_SYS_CLK_FREQ * 10 kHz). This is measured once after any reset, including GBC_BRD_RST. This value is not available (will read 0) until 100us after reset.

### 6.1.7 GBC_USER_ID (READ ONLY)

This value is set by jumpers on the board, and is used to identify individual board when there are multiple in the same system.

### 6.1.8 GBC_IRQ_STATUS (READ/CLEAR)

This is a 64-bit interrupt status register for non-DMA interrupts. Each bit in this register corresponds to one of the Function Blocks; bit 0 corresponds to FB0 (whose ID and OFFSET are at 0x020), etc. Bits 60 through 63 are reserved. This is a "sticky" register, and the driver clears it by writing a '1' to the appropriate bit. The interrupts signaled by this registered are generally handled by a User Mode Delayed Procedure Call. Any status information required to service the interrupt must be latched in the Function Block. This typically means that there will also be a sticky status register in the Function Block.

The Interrupt Service Routing must be able to clear the interrupt without accessing any registers in the Function Block. This means that if a persistent interrupt condition occurs (i.e. FIFO Empty) the GBC_IRQ_STATUS register will initially be set. The ISR will then clear the bit in GBC_IRQ_STATUS and launch the DPC. In this state the interrupt condition still exists, but the status bit is cleared (because we are servicing it). Depending on implementation, that Function Block may not be able to issue another interrupt while in this state. In this state the full status of the board cannot be determined just from the GBC_IRQ_STATUS register. The Function Block should also maintain a status register that will indicate if the interrupt condition still exists, which will be cleared by the DPC. By doing an End-Of-Interrupt (see Section 6.1.10 GBC_EOI (Read/Clear) below) any "hidden" interrupts will be generated again.

### 6.1.9 GBC_DIRQ_STATUS (READ/CLEAR)

This is a 64-bit interrupt status register for DMA interrupts. Each bit in this register corresponds to one of the Function Blocks; bit 0 corresponds to FB0 (whose ID and OFFSET are at 0x020), etc. Bits 60 through 63 are reserved. This is a "sticky" register, and the driver clears it by writing a '1' to the appropriate bit. The interrupts signaled by this registered are generally handled by the Kernel Mode ISR. This interrupt is only for the Function Block Standard DMA in Section 6.2 on page 41.

### 6.1.10 GBC_EOI (READ/CLEAR)

This register is used to acknowledge an interrupt. It is used to safeguard against missing an interrupt. At the end of the ISR, write a 0x01 to this register. If there is another interrupt pending in the status registers, the interrupt line is toggled (Legacy Mode), or another interrupt is sent (MSI Mode).

### 6.1.11 FBN_ID (READ-ONLY)

This is a 32-bit value that identifies the type of Function Block in slot 'n'. Any changes to a Function Block result in a new Block ID. The mappings for the Functional Block ID can be found on page 38. The ID consists of three fields:

- B[31:24] Type Revision – This is used to indicate the addition of features to the function block. Any checks in the software should be of the form (Type Revision > NN) so that the driver doesn't fail with a newer FPGA. Any changes to the FPGA that would break existing software must change the Type, not the Type Revision.
- B[23:16] Subtype – A Subtype is a variant of the Type with one of the following differences. This allows the driver and library to use the same functions, but have different enumerations.
- B[15:0] Type – The Type of the Function Block is used to define the register map. Any time that the positions of registers change, or registers are added or removed require a new Type number. This is loosely separated into
    - B[15:8] Family – i.e. ADC, DAC, Digital I/O, etc.
    - B[7:0] Member

### 6.1.12 FBN_OFFSET (READ-ONLY)

This is the offset from the beginning of the Functional Block section (typically the offset in BAR2) that this Functional Block resides in.

### 6.1.13 FBN_OFFSET_DMA (READ-ONLY)

This is the offset from the beginning of the Functional Block section (typically the offset in BAR2) that the Functional Block DMA Registers resides in.

## 6.2 BAR2: Functional Block Standard DMA

This section describes a standard DMA engine implementation that may be used by the Functional Blocks. Any Functional Block that uses DMA shall use this implementation so that the kernel mode driver may be used to service it, resulting in better performance.

***Table 24: DMA Registers***

| Offset | 0x03 | 0x02 | 0x01 | 0x00 |
|---|---|---|---|---|
| D + 0x00 | FB_DMAm_Stat_Underflow | FB_DMAm_Stat_Overflow | FB_DMAm_Setup | FB_DMAm_Action |
| D + 0x04 | FB_DMAm_Current_Buffer | FB_DMAm_Count | | |
| D + 0x08 | FB_DMAm_RD_FIFO_CNT | | FB_DMAm_WR_FIFO_CNT | |
| D + 0x0C | FB_DMAm_Last_Action | FB_DMAm_Stat_Complete | FB_DMAm_Stat_Invalid | FB_DMAm_Stat_Used |
| D + 0x10 | FB_DMAm_CTRL0 | FB_DMAm_STAT0 | Reserved | |
| D + 0x14 | Reserved | FB_DMAm_SIZE0 | | |
| D + 0x18 | FB_DMAm_ADDRESS0 | | | |
| D + 0x1C | | | | |
| D + 0x20 | FB_DMAm_CTRL1 | FB_DMAm_STAT1 | Reserved | |
| D + 0x24 | Reserved | FB_DMAm_SIZE1 | | |
| D + 0x28 | FB_DMAm_ADDRESS1 | | | |
| D + 0x2C | | | | |
| … | | | | |
| D + 0x10 + (0x10 * n) | FB_DMAm_CTRLn | FB_DMAm_STATn | Reserved | |
| D + 0x14 + (0x10 * n) | Reserved | FB_DMAm_SIZEn | | |
| D + 0x18 + (0x10 * n) | FB_DMAm_ADDRESSn | | | |
| D + 0x1C + (0x10 * n) | | | | |

### 6.2.1 FB_DMAm_Action (Read/Write)

After writing to the Action register, the user should poll the Last_Action register (below) until it reads the same value. This shows that the action has been performed by the DMA state machine. This is especially important when entering and exiting the Clear state.

- 0x00 = Clear: Clear the Current Buffer field, the internal offset counters, and the FIFO. DMA is stopped.
- 0x01 = Go: Starts DMA
- 0x02 = Pause: DMA transfers are stopped, but all internal registers maintain their state. During PAUSE you will still receive Stat_Underflow and Stat_Overflow interrupts. After PAUSE, you may transition to GO or CLEAR.
- 0x03 = Halt: Buffer has been filled that has the HALT bit set, or has attempted to use a buffer with the Valid bit cleared. After HALT, you must transition to CLEAR.

### 6.2.2 FB_DMAm_Last_Action (Read/Write)

The DMA Engine writes the value of FB_DMAm_Action to this register after it has completed this channel. This indicates to the user that the last command has been processed. It specifically aids the transition to Clear. When transitioning to Clear, the user should wait until FB_DMAm_Last_Action indicates that the Clear has been processed before allowing any other Action changes.

The user may also write a value to this register and then poll the register to see when the value changes. This method can be used to detect when the DMA engine services the channel without an Action change.

### 6.2.3 FB_DMAm_Setup (Read/Write)

- B0:IntEna: Set to '1' to enable the DMA engine to generate interrupts on completion of a buffer.
- B1:ErrIntEna: Set to '1' to enable the DMA engine to generate interrupts on error.
- B2:Direction (RO or R/W): Set to '1' to transfer from the FPGA to the PCI bus. Clear to '0' to transfer from the PCI bus to the FPGA.
- B3:IgnoreUsed: Set to '1' to prevent an error condition when accessing a buffer with the Used bit set. When "IgnoreUsed" is set, the hardware will still set the Used_Desc bit (below) if the next buffer has the Used bit set. However, it will not generate an interrupt, and will not PAUSE the DMA engine. Examples are continuous output from a DAC, or very large Pre-trigger buffering using system memory.

### 6.2.4 FB_DMAm_Stat_Used (Read/Write)

This register is used to determine the source of a DMA interrupt. The bits are cleared by writing 0x00 to the byte. Stat_Used will be set regardless of having ErrIntEna set to '1', and regardless of the state of the IgnoreUsed bit (above).

- B0: Used_Desc (R/C). Set to '1' by the DMA engine if it attempting to use a descriptor with the Used bit set.

### 6.2.5 FB_DMAm_Stat_Invalid (Read/Write)

This register is used to determine the source of a DMA interrupt. The bits are cleared by writing 0x00 to the byte. Stat_Invalid will be set regardless of having ErrIntEna set to '1'.

- B0: Invalid_Desc (R/C). Set to '1' by the DMA engine if it attempting to use a descriptor with the Valid bit cleared.

### 6.2.6 FB_DMAm_Stat_Overflow (Read/Write)

This register is used to determine the source of a DMA interrupt. The bits are cleared by writing 0x00 to the byte. Stat_Overflow will be set regardless of having ErrIntEna set to '1'.

- B0: Overflow (R/C). Set to '1' by the DMA engine if an overflow occurred on the FIFO.

### 6.2.7 FB_DMAm_Stat_Underflow (Read/Write)

This register is used to determine the source of a DMA interrupt. The bits are cleared by writing 0x00 to the byte. Stat_Underflow will be set regardless of having ErrIntEna set to '1'.

- B0: Underflow (R/C). Set to '1' by the DMA engine if an underflow occurred on the FIFO.

### 6.2.8 FB_DMAm_Stat_Complete (Read/Write)

This register is used to determine the source of a DMA interrupt. The bits are cleared by writing 0x00 to the byte.

- B0: Buffer_Complete (R/C). Set to '1' by the DMA engine when a buffer is filled that has the Interrupt bit set.

### 6.2.9 FB_DMAm_Current_Buffer (Read-Only)

This is the ID for the buffer that will be used for the next access. The user may use this to track the progress of the DMA activity.

### 6.2.10 FB_DMAm_COUNT (Read-Only)

This is the offset in the DMA buffer for the next access. The user may use this to track the progress of the DMA activity.

### 6.2.11 FB_DMAm_RD_FIFO_CNT(Read-Only)

- B[9:0] This is the amount of data available in the read FIFO in bytes. Software can use this to determine when the FIFO is empty. A value of 0x3FC indicates that there are 1020 or more bytes available.
- B15: RD_EMPTY- '1' indicates that the read FIFO is empty

### 6.2.12 FB_DMAm_WR_FIFO_CNT(Read-Only)

- B[9:0] This is the amount of space available in the write FIFO in bytes. Software can use this to determine when the FIFO is empty. A value of 0x3FC indicated that there are 1020 or more bytes available.
- B15: WR_FULL- '1' indicates that the read FIFO is full

### 6.2.13 FB_DMAm_ADDRESSn (Read/Write)

This is the 64-bit PCI address for DMA Channel m, buffer n. It must be double-word aligned (i.e. b[1:0] are reserved).

### 6.2.14 FB_DMAm_SIZEn (Read/Write)

This is the size in bytes of the buffer for DMA Channel m, buffer n. It must be an integer number of double-words (i.e. b[1:0] are reserved). The actual size is FB_DMAm_SIZEn + 4 Bytes. The maximum buffer size is 16MB.

### 6.2.15 FB_DMAM_CTRLN (READ/WRITE)

- B0: Valid: Sets this bit to '1' to indicate that this contains valid information. The DMA engine will set the error bit and halt if it is ready to use this descriptor and it is not valid.
- B1: Halt: Sets this bit to '1' to halt the DMA engine after this buffer is full.
- B2: Loop: Sets this bit to '1' to start back at descriptor 0 after this buffer is full. This has a higher priority than the HALT bit.
- B3: Interrupt: Sets this bit to '1' to generate an interrupt after this buffer is full.
- B4: Pause: Sets this bit to '1' to pause the DMA engine after this buffer is full.

If the last buffer is reached, and the HALT and LOOP bits are both '0', the DMA engine will loop.

If the last buffer is reached, and the HALT and LOOP bits are both '1', the DMA engine will halt and the Current_Buffer will be set to 0.

### 6.2.16 FB_DMAM_STATN (READ/CLEAR)

- B0: Used (R/C): DMA engine sets to '1' to indicate that it has completely used this descriptor. The user must clear this bit when it is ready to be used again. The DMA engine will set the error bit and PAUSE if it is ready to use this descriptor and the Used bit is set, unless the IgnoreUsed bit is set. The bits are cleared by writing 0x00 to the byte.
- B1: Terminated (R/C): DMA engine sets to '1' to indicate that this buffer was terminated early at the request of the associated Function Block.

## 6.3 BAR2: Functional Block Header Registers

Each Functional Block has a standard header as follows.

***Table 25: Functional Block Header***

| Offset | 0x03 | 0x02 | 0x01 | 0x00 |
|---|---|---|---|---|
| FB + 0x00 | FB_ID | | | |
| FB + 0x04 | FB_DMA_BUFFERS | FB_DMA_CHANNELS | Reserved | Reserved |

### 6.3.1 FB_ID (READ-ONLY)

This is a repeat of the ID from the General Board Control section. This can be used to validate that the correct Function Block is being accessed.

### 6.3.2 FB_DMA_CHANNELS (READ -ONLY)

This register contains the number of DMA Channels in this Function Block.

### 6.3.3 FB_DMA_BUFFERS (READ-ONLY)

This register contains the number of Buffer Descriptors in each DMA Channel.

## 6.4 BAR2: Analog to Digital Converter (ADC)

This Function Block is for an Analog to Digital converter. The DM35418 has eight ADC Function blocks, one for each of the eight ADC inputs. The ADC0 input is associated with the lowest-numbered ADC Function Block, and ADC7 is associated with the highest-numbered ADC Function Block. Each Function Block has its own clock, triggers, and DMA channel.

This Function Block is for an Analog to Digital converter. The DM35218 has four ADC Function blocks, one for each of the four ADC inputs. The ADC0 input is associated with the lowest-numbered ADC Function Block, and ADC3 is associated with the highest-numbered ADC Function Block. Each Function Block has its own clock, triggers, and DMA channel.

### 6.4.1 Function Block Register Map

***Table 26: Multi-Channel A/D Functional Block***

| | Offset | 0x03 | 0x02 | 0x01 | 0x00 |
|---|---|---|---|---|---|
| Header | FB + 0x00 | FB_ID | | | |
| | FB + 0x04 | FB_DMA_BUFFERS | FB_DMA_CHANNELS | Reserved | *Reserved* |
| ADC Control | FB + 0x08 | STOP_TRIG | START_TRIG | CLK_SRC | MODE_STATUS |
| | FB + 0x0C | CLK_DIV | | | |
| | FB + 0x10 | CLK_DIV_CNTR | | | |
| | FB + 0x14 | PRE_TRIGGER_CAPTURE (limited by FIFO size) | | | |
| | FB + 0x18 | POST_STOP_CAPTURE | | | |
| | FB + 0x1C | SAMPLE_CNT | | | |
| | FB + 0x20 | INT_ENA (Sample, Start, Stop, Threshold, Pacer Tick, etc) | | | |
| | FB + 0x24 | INT_STAT | | *Reserved* | |
| | FB + 0x28 | CLK_BUS3 | CLK_BUS2 | | *Reserved* |
| | FB + 0x2C | CLK_BUS7 | CLK_BUS6 | CLK_BUS5 | CLK_BUS4 |
| | FB + 0x30 | AD_CONFIG (Maskable register – 16-bit) | | | |
| ADC Channel | FB + 0x34 | CH_FRONT_END_CONFIG (Maskable register – 16-bit) | | | |
| | FB + 0x38 | CH_FIFO_DATA_CNT | | | |
| | FB + 0x3C | CH_INT_ENA | CH_INT_STAT | CH_FILTER | *Reserved* |
| | FB + 0x40 | CH_THRESH_LOW | | | |
| | FB + 0x44 | CH_THRESH_HIGH | | | |
| | FB + 0x48 | CH_LAST_SAMPLE | | | |
| FIFO | FB + 0x4C | CH_FIFO_ACCESS | | | |

### 6.4.2 Mode_Status (Read/Write, Read-Only)

Selects the current mode of operation and indicates its triggering status.

B[3:0]: Mode

- 0x04: Uninitialized. This is the power-on state. No converter initialization has taken place. Sampling is stopped, and all counters are reset and the triggering state machine is reset. Transition to any of the other Modes will start converter initialization (sampling will not start until initialization is complete).
- 0x00: Reset. Sampling is stopped. All counters are reset and the triggering state machine is reset.
- 0x01: Paused. Sampling is stopped, but the counters and triggering state machine maintain their state.
- 0x02: Go, Single-Shot. After filling the buffer with the Post-Stop samples, capturing stops. The Mode must be set back to RESET in order to capture more samples.
- 0x03: Go, Re-arm. After filling the buffer with the Post-Stop samples and the FIFO is empty, the triggering state machine is restarted, i.e. FIFO is filled with Pre-Start samples and waits for a start trigger.

B[7:4]: Status

- 0x08: Uninitialized – The status when in the “Uninitialized” mode and the converter requires initialization.
- 0x09: Initializing
- 0x00: Stopped – The status when in the “Reset” mode, or in the “Uninitialized” mode and the converter does not require initialization.
- 0x01: Filling Pre-Trigger buffer
- 0x02: Waiting for start trigger
- 0x03: Sampling/Waiting for stop trigger
- 0x04: Filling Post-Stop buffer
- 0x05: Wait to re-arm – Waiting until local FIFO is empty so the pre-trigger buffer can be filled.
- 0x07: Done capturing

### 6.4.3 CLK_SRC (READ/WRITE)

Selects the source for CLK_DIV from the clock bus.

Below is the list of clock sources and the register value needed to select the source.

B[7:0]:

- 0x00: System clock/immediate
- 0x01: Never
- 0x02: CLK_BUS2
- 0x03: CLK_BUS3
- 0x04: CLK_BUS4
- 0x05: CLK_BUS5
- 0x06: CLK_BUS6
- 0x07: CLK_BUS7
- 0x08: Channel Threshold – One of the channels has exceeded the High or Low threshold.
- 0x09: Channel Threshold Inverted– All of the channels are within the High and Low threshold.
- 0x0A: CLK_BUS2 Inverted
- 0x0B: CLK_BUS3 Inverted
- 0x0C: CLK_BUS4 Inverted
- 0x0D: CLK_BUS5 Inverted
- 0x0E: CLK_BUS6 Inverted
- 0x0F: CLK_BUS7 Inverted

### 6.4.4 START_TRIG (READ/WRITE)

Selects the start trigger from the clock bus. CLK_DIV will start counting after the start trigger, unless PRE_TRIGGER_CAPTURE is non-zero in which case CLK_DIV will start counting immediately.

Refer to CLK_SRC (Read/Write) section above, for list of valid values.

### 6.4.5 STOP_TRIG (READ/WRITE)

Selects the stop trigger from the clock bus.

Refer to CLK_SRC (Read/Write) section above, or list of valid values..

### 6.4.6 CLK_DIV (READ/WRITE)

Divider for the pacer clock. Pacer Clock Frequency = (Clk_Src_Frequency) / (1 + CLK_DIV). If synchronizing with the pacer clock from another Function Block (by using one of the CLK_BUS signals), this is typically set to 0.

### 6.4.7 CLK_DIV_CNTR (READ ONLY)

The current value of the Clock Divide Counter. This counter starts at a value of CLK_DIV, and counts down. When it reaches zero, a sample is taken. This is useful when using a slow sample clock.

### 6.4.8 PRE_TRIGGER_CAPTURE (READ/WRITE)

Number of samples to collect before the Start Trigger. The length is limited by the FIFO size – writing a value larger than the FIFO size will have indeterminate results.

### 6.4.9 POST_STOP_CAPTURE (READ/WRITE)

Number of samples to collect after the Stop Trigger.

### 6.4.10 SAMPLE_CNT (READ ONLY)

Total number of samples collected. This does not increment in while in the "Waiting For Start Trigger" state. It also continues counting after a Re-Arm.

### 6.4.11 INT_ENA (MASKABLE READ/WRITE)

Each bit corresponds to an interrupt source. A value of '1' enables the source, and a value of '0' disables it. See below for a description of the sources.

### 6.4.12 INT_STAT (READ/CLEAR)

Each bit corresponds to an interrupt source. Reading a value of '1' indicates that an event has occurred. Reading a value of '0' indicates that the event has not occurred. Writing a '1' will clear that bit.

B0: Sample – A sample has been taken.

B1: Channel Threshold – One of the channels has exceeded the High or Low threshold. Check the CH_THRESH_STAT registers.

B2: Pre-Start Buffer Filled

B3: Start Trigger

B4: Stop Trigger

B5: Post-Stop Buffer Filled

B6: Sampling has completed and the FIFO is empty (all data transferred to host)

B7: Pacer – The pacer clock has ticked.

### 6.4.13 CLK_BUSN

***NOTE: If a CLK_BUS is unassigned in all function blocks, it defaults to System Clock/Immediate.***

Selects the source to drive onto Clock Bus signal N.

B[7:0]:

- 0x00: Disables Clock Source
- 0x80: Sample – A sample has been taken.
- 0x81: Channel Threshold – One of the channels has exceeded the High or Low threshold. Check the CH_THRESH_STAT registers.
- 0x82: Pre-Start Buffer Filled
- 0x83: Start Trigger
- 0x84: Stop Trigger
- 0x85: Post-Stop Buffer Filled
- 0x86: Sampling has completed and the FIFO is empty (all data transferred to host)
- 0x87: Pacer – The pacer clock has ticked.

### 6.4.14 AD_CONFIG (MASKABLE READ/WRITE)

Not used.

### 6.4.15 CH_FRONT_END_CONFIG (MASKABLE READ/WRITE)

Refer to section 5.6.2 for more information about the front end circuit.

This register provides configuration to the Front End for this ADC Channel.

B[5]: G_05_1 – 0 = gain *0.5 selected, 1 = gain *1 selected
B[4]: PGA_A1
B[3]: PGA_A0

- PGA_A[1:0] = 00: Gain of 1
- PGA_A[1:0] = 01: Gain of 2
- PGA_A[1:0] = 10: Gain of 4
- PGA_A[1:0] = 11: Gain of 8

B[2]: BIP_UNI 0 = bipolar operation 1 = unipolar operation
B[1:0]: MODE

- 00 = input connected to +5V VREF
- 01 = single ended operation
- 11 = differential operation

### 6.4.16 CHN_FIFO_DATA_CNT (READ)

This register shows the current sample count that is available in the ADC channel FIFO.

### 6.4.17 CH_FILTER (READ/WRITE)

The programmable digital filter provides a single pole Infinite Impulse Response (IIR) filter on each channel. This a unity-gain filter. The filtered data has a value of:

$$D_n = \frac{D_{n-1} \times (2^{ORDER} - 1) + NewSample}{2^{ORDER}}$$

The response of the filter is shown in the Figure 16below. The Table below shows the -3dB cutoff for each of the filter settings. Both the figure and the table are relative to the sample rate ($f_s$).

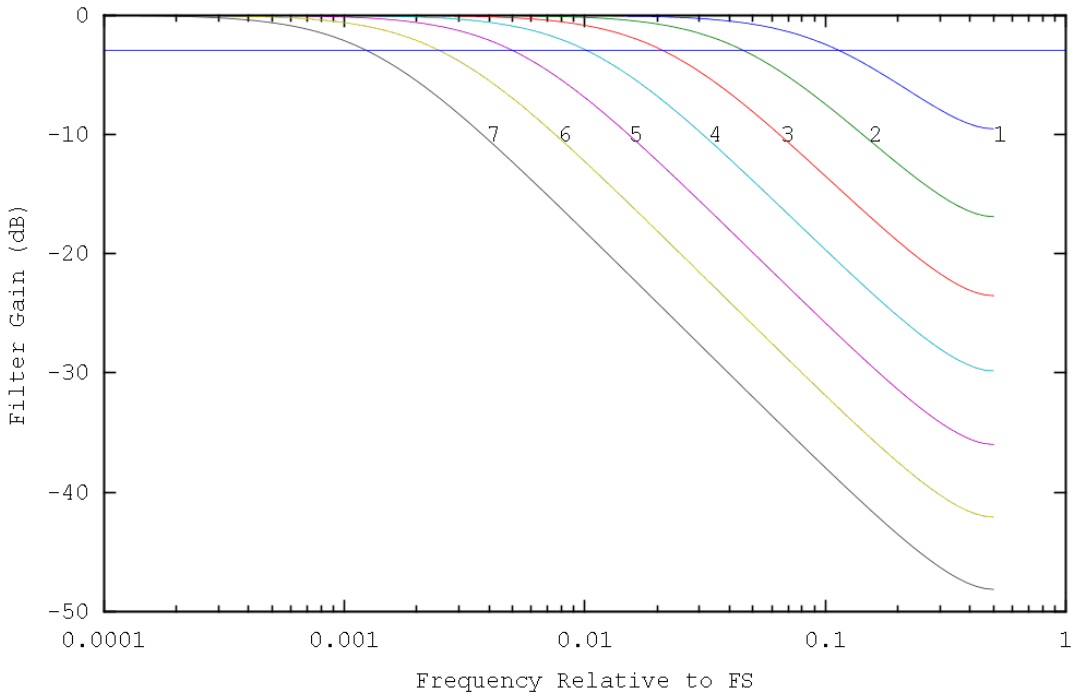



***Figure 16: Filter Response with each ORDER Value***

| ORDER | -3 dB Cutoff |
|---|---|
| 0 | n/a |
| 1 | 0.114791 * $f_s$ |
| 2 | 0.045995 * $f_s$ |
| 3 | 0.021236 * $f_s$ |
| 4 | 0.010255 * $f_s$ |
| 5 | 0.005042 * $f_s$ |
| 6 | 0.002501 * $f_s$ |
| 7 | 0.001246 * $f_s$ |

### 6.4.18 CH_INT_STAT(READ/CLEAR)

This is the status register for the channel interrupts. Reading a value of '1' indicates that an event has occurred. Reading a value of '0' indicates that the event has not occurred. Writing a '1' will clear that bit.

B0: '1' = Low Threshold has been crossed
B1: '1' = High Threshold has been crossed

### 6.4.19 CH_INT_ENA (READ/WRITE)

This is the interrupts enable for the threshold detection. Bit defines are above. An interrupt is generated (if not already generated) each time a sample is taken and the value is above the high threshold or below the low threshold.

### 6.4.20 CH_THRESH_LOW (READ/WRITE)

Signed 32-bit value indicating the low threshold. If the input signal drops below this value, an interrupt or clock can be generated until the signal goes above this value. The 3 least significant bits are ignored from the actual threshold value.

***NOTE: The threshold value should not exceed the ADC range. If the threshold value exceeds the ADC range unexpected results will occur.***

### 6.4.21 CH_THRESH_HIGH (READ/WRITE)

Signed 32-bit value indicating the high threshold. If the input signal goes above this value, an interrupt or clock can be generated until the signal goes below this value. The 3 least significant bits are ignored from the actual threshold value.

***NOTE: The threshold value should not exceed the ADC range. If the threshold value exceeds the ADC range unexpected results will occur.***

### 6.4.22 CH_LAST_SAMPLE (READ-ONLY)

The last sample read from the ADC Converter, after filtering. This is the same value that is written to the DMA FIFO.

## 6.5 BAR2: Digital to Analog Converter (DAC)

This Function Block is for a Digital to Analog converter. The DM35418 has eight DAC Function blocks, one for each of the eight DAC outputs. The DAC0 output is associated with the lowest-numbered DAC Function Block, and DAC7 is associated with the highest-numbered DAC Function Block. Each Function Block has its own clock, triggers, and DMA channel.

This Function Block is for a Digital to Analog converter. The DM35218 has four DAC Function blocks, one for each of the four DAC outputs. The DAC0 output is associated with the lowest-numbered DAC Function Block, and DAC3 is associated with the highest-numbered DAC Function Block. Each Function Block has its own clock, triggers, and DMA channel.

### 6.5.1 FUNCTION BLOCK REGISTER MAP

***Table 27: Multi-Channel DAC Functional Block***

| | Offset | 0x03 | 0x02 | 0x01 | 0x00 |
|---|---|---|---|---|---|
| Header | FB + 0x00 | FB_ID | | | |
| | FB + 0x04 | FB_DMA_BUFFERS | FB_DMA_CHANNELS | *Reserved* | *Reserved* |
| DAC Control | FB + 0x08 | STOP_TRIG | START_TRIG | CLK_SRC | MODE_STATUS |
| | FB + 0x0C | CLK_DIV | | | |
| | FB + 0x10 | CLK_DIV_CNTR | | | |
| | FB + 0x14 | Reserved | | | |
| | FB + 0x18 | POST_STOP_CONVERSIONS | | | |
| | FB + 0x1C | CONVERSION_CNT | | | |
| | FB + 0x20 | INT_ENA (Conversion, Start, Stop, Error, Channel) | | | |
| | FB + 0x24 | INT_STAT | | *Reserved* | |
| | FB + 0x28 | CLK_BUS3 | CLK_BUS2 | | *Reserved* |
| | FB + 0x2C | CLK_BUS7 | CLK_BUS6 | CLK_BUS5 | CLK_BUS4 |
| | FB + 0x30 | DA_CONFIG (Maskable register – 16-bit) | | | |
| DAC Channel | FB + 0x34 | CH_FRONT_END_CONFIG (Maskable register – 16-bit) | | | |
| | FB + 0x38 | CH_FIFO_DATA_CNT | | | |
| | FB + 0x3C | CH_INT_ENA | CH_INT_STAT | *Reserved* | *Reserved* |
| | FB + 0x40 | *Reserved (Checksum of DAC Data)* | | | |
| | FB + 0x44 | CH_LAST_CONVERSION | | | |
| FIFO | FB + 0x48 | CH_FIFO_ACCESS | | | |

### 6.5.2 MODE_STATUS (READ/WRITE, READ-ONLY)

Selects the current mode of operation and indicates its triggering status.

B[3:0]: Mode

- 0x04: Uninitialized. This is the power-on state. No converter initialization has taken place. Sampling is stopped, and all counters are reset and the triggering state machine is reset. Transition to any of the other Modes will start converter initialization (sampling will not start until initialization is complete).
- 0x00: Reset. Sampling is stopped. All counters are reset and the triggering state machine is reset.
- 0x01: Paused. Sampling is stopped, but the counters and triggering state machine maintain their state.
- 0x02: Go, Single-Shot. After converting the Post-Stop number of values, converting stops. The Mode must be set back to RESET in order to convert more values.
- 0x03: Go, Re-arm. After converting the Post-Stop number of values, the triggering state machine is restarted. DAC data is resumed from that last value sent.

B[7:4]: Status

- 0x08: Uninitialized – The status when in the "Uninitialized" mode and the converter requires initialization.
- 0x09: Initializing
- 0x00: Stopped – The status when in the "Reset" mode, or in the "Uninitialized" mode and the converter does not require initialization.
- 0x01: *Reserved*
- 0x02: Waiting for start trigger
- 0x03: Converting/Waiting for stop trigger
- 0x04: Output Post-Stop buffer
- 0x05: Wait to re-arm
- 0x07: Done capturing

### 6.5.3 CLK_SRC (READ/WRITE)

Selects the source for CLK_DIV from the clock bus.

Below is the list of clock sources and the register value needed to select the source.

B[7:0]:

- 0x00: System clock/immediate
- 0x01: Never
- 0x02: CLK_BUS2
- 0x03: CLK_BUS3
- 0x04: CLK_BUS4
- 0x05: CLK_BUS5
- 0x06: CLK_BUS6
- 0x07: CLK_BUS7
- 0x08: Channel Marker – One of the channels has an enabled marker.
- 0x09: Channel Marker Inverted– No enabled markers are asserted.
- 0x0A: CLK_BUS2 Inverted
- 0x0B: CLK_BUS3 Inverted
- 0x0C: CLK_BUS4 Inverted
- 0x0D: CLK_BUS5 Inverted
- 0x0E: CLK_BUS6 Inverted
- 0x0F: CLK_BUS7 Inverted

### 6.5.4 START_TRIG (READ/WRITE)

Selects the start trigger from the clock bus. CLK_DIV will start counting after the start trigger.

Refer to CLK_SRC (Read/Write) section above, for list of valid values.

### 6.5.5 STOP_TRIG (READ/WRITE)

Selects the stop trigger from the clock bus.

Refer to CLK_SRC (Read/Write) section above, for list of valid values.

### 6.5.6 CLK_DIV (READ/WRITE)

Divider for the pacer clock. Pacer Clock Frequency = (Clk_Src_Frequency) / (1 + CLK_DIV). If synchronizing with the pacer clock from another Function Block (by using one of the CLK_BUS signals), this is typically set to 0.

### 6.5.7 CLK_DIV_CNTR (READ ONLY)

The current value of the Clock Divide Counter. This counter starts at a value of CLK_DIV, and counts down. When it reaches zero, a sample is taken. This is useful when using a slow sample clock.

### 6.5.8 POST_STOP_CONVERSIONS (READ/WRITE)

Number of conversions to send after the Stop Trigger.

### 6.5.9 CONVERSION_CNT (READ ONLY)

Total number of conversions. It also continues counting after a Re-Arm.

### 6.5.10 INT_ENA (MASKABLE READ/WRITE)

Each bit corresponds to an interrupt source. A value of '1' enables the source, and a value of '0' disables it. See below for a description of the sources.

### 6.5.11 INT_STAT (READ/CLEAR)

Each bit corresponds to an interrupt source. Reading a value of '1' indicates that an event has occurred. Reading a value of '0' indicates that the event has not occurred. Writing a '1' will clear that bit.

B[0]: Conversion – A value has been sent.
B[1]: Channel Marker – One of the channels has an enabled marker.
B[2]: Reserved
B[3]: Start Trigger
B[4]: Stop Trigger
B[5]: Post-Stop Conversions Completed

### 6.5.12 CLK_BUSN

***NOTE: If a CLK_BUS is unassigned in all function blocks, it defaults to System Clock/Immediate.***

Selects the source to drive onto Clock Bus signal N.

B[7:0]:

- 0x00: Disable Clock Source
- 0x80: Conversion – A value has been sent.
- 0x81: Channel Marker – One of the channels has an enabled marker.
- 0x82: Reserved
- 0x83: Start Trigger
- 0x84: Stop Trigger
- 0x85: Post-Stop Conversions Completed

### 6.5.13 DA_CONFIG (MASKABLE READ/WRITE)

Not used.

### 6.5.14 CH_FRONT_END_CONFIG (MASKABLE READ/WRITE)

This register provides configuration to the Front End for this DAC Channel.

B[1:0]: PGA_A[1:0]

- PGA_A[1:0]: 00: Gain of 1
- PGA_A[1:0]: 01: Gain of 2
- PGA_A[1:0]: 10: Gain of 4

***Table 28: DAC Full-Scale Settings***

| PGA_A[1:0] | Gain | Range |
|---|---|---|
| 00 | 1 | ±2.5V |
| 01 | 2 | ±5V |
| 10 | 4 | ±10V |

### 6.5.15 CHN_FIFO_DATA_CNT (READ)

This register shows the current sample count that is available in the ADC channel FIFO.

### 6.5.16 CH_INT_STAT (READ/CLEAR)

This is the status register for the channel interrupts. Reading a value of '1' indicates that an event has occurred. Reading a value of '0' indicates that the event has not occurred. Writing a '1' will clear that bit.

The upper eight bits of the DAC value can be used for Markers. These Markers can be used to generate an interrupt when a certain part of the waveform is sent to the DAC. This allows an automated indication to the application software as to the state of the data being sent to the DAC. Marker bit 7 corresponds to bit 31 of the DAC data, and Marker bit 0 corresponds to bit 24 of the DAC data.

B0: Marker 0
B1: Marker 1
B2: Marker 2
B3: Marker 3
B4: Marker 4
B5: Marker 5
B6: Marker 6
B7: Marker 7

### 6.5.17 CH_INT_ENA (READ/WRITE)

These are interrupts enables for the Data Markers. Bit defines are above.

### 6.5.18 CH_LAST_CONVERSION (READ/WRITE)

The last value sent to the DAC Converter.

B[31:24]: DAC Markers
B[15:0]: DAC Data

If the current Mode is "Reset" or the associated DMA engine is set to "Clear", a write to this register will immediately update the DAC Converter.

## 6.6 BAR2: Digital I/O (DIO)

This function block is for 32 bi-directional digital I/O. There are not any interrupts or DMA.

### 6.6.1 FUNCTION BLOCK REGISTER MAP

***Table 29: Digital I/O Functional Block***

| | Offset | 0x03 | 0x02 | 0x01 | 0x00 |
|---|---|---|---|---|---|
| Header | FB + 0x00 | FB_ID | | | |
| | FB + 0x04 | FB_DMA_BUFFERS | FB_DMA_CHANNELS | *Reserved* | *Reserved* |
| DIO Control | FB + 0x08 | DIO_INPUT_VAL | | | |
| | FB + 0x0C | DIO_OUTPUT_VAL | | | |
| | FB + 0x10 | DIO_DIRECTION | | | |

### 6.6.2 DIO_INPUT_VAL (READ ONLY)

This register provides the current value on the Digital I/O lines. The bits in the register correspond with the Digital I/O pins as follows:

| Bit | CN3 Pin Number | Signal Name |
|---|---|---|
| 31 | 34 | DIO0.31 |
| 30 | 33 | DIO0.30 |
| 29 | 32 | DIO0.29 |
| 28 | 31 | DIO0.28 |
| 27 | 30 | DIO0.27 |
| 26 | 29 | DIO0.26 |
| 25 | 28 | DIO0.25 |
| 24 | 27 | DIO0.24 |
| 23 | 26 | DIO0.23 |
| 22 | 25 | DIO0.22 |
| 21 | 24 | DIO0.21 |
| 20 | 23 | DIO0.20 |
| 19 | 22 | DIO0.19 |
| 18 | 21 | DIO0.18 |
| 17 | 20 | DIO0.17 |
| 16 | 19 | DIO0.16 |

| Bit | CN3 Pin Number | Signal Name |
|---|---|---|
| 15 | 16 | DIO0.15 |
| 14 | 15 | DIO0.14 |
| 13 | 14 | DIO0.13 |
| 12 | 13 | DIO0.12 |
| 11 | 12 | DIO0.11 |
| 10 | 11 | DIO0.10 |
| 9 | 10 | DIO0.9 |
| 8 | 9 | DIO0.8 |
| 7 | 8 | DIO0.7 |
| 6 | 7 | DIO0.6 |
| 5 | 6 | DIO0.5 |
| 4 | 5 | DIO0.4 |
| 3 | 4 | DIO0.3 |
| 2 | 3 | DIO0.2 |
| 1 | 2 | DIO0.1 |
| 0 | 1 | DIO0.0 |

### 6.6.3 DIO_OUTPUT_VAL (READ/WRITE)

The value to be output if the pins are configured as output. Bit assignments are the same as above.

### 6.6.4 DIO_DIRECTION (READ/WRITE)

Selects the direction of the I/O bit. 0=input, 1=output. Bit assignments are the same as above.

All pins default to inputs at power-up.

## 6.7 BAR2: Temperature Sensor

This function block provides readout of the onboard temperature sensor. There are not any interrupts or DMA.

### 6.7.1 FUNCTION BLOCK REGISTER MAP

***Table 30: Temperature Sensor Functional Block***

| | Offset | 0x03 | 0x02 | 0x01 | 0x00 |
|---|---|---|---|---|---|
| Header | FB + 0x00 | FB_ID | | | |
| | FB + 0x04 | FB_DMA_BUFFERS | FB_DMA_CHANNELS | Reserved | *Reserved* |
| | FB + 0x08 | *Reserved* | | TEMPERATURE_VAL | |

### 6.7.2 TEMPERATURE_VAL (READ ONLY)

The current value on the temperature sensor as a signed 16-bit integer. B[2:0] of this register always read '0'. See the equation and table below for converting register value to temperature.

$$Temperature = Register\ Value * 0.0078125\ C$$

| Temperature (ºC) | Register Value |
|---|---|
| 150 | 0x4B00 |
| 125 | 0x3E80 |
| 25 | 0x0C80 |
| 0.0625 | 0x0008 |
| 0 | 0x0000 |
| -0.0625 | 0xFFF8 |
| -25 | 0xF380 |
| -55 | 0xE480 |

## 6.8 BAR2: SyncBus Driver

This function block provides an interface to the SyncBus. It is used clock synchronization between multiple boards.

### 6.8.1 FUNCTION BLOCK REGISTER MAP

***Table 31: SyncBus Functional Block***

| | Offset | 0x03 | 0x02 | 0x01 | 0x00 |
|---|---|---|---|---|---|
| Header | FB + 0x00 | FB_ID | | | |
| | FB + 0x04 | FB_DMA_BUFFERS | FB_DMA_CHANNELS | *Reserved* | *Reserved* |
| SyncBus Control | FB + 0x08 | ENABLE | TERM_ENABLE | PLL_LOCKED | CLK_SEL |
| | FB + 0x0C | DIRECTION | SB_2_CLK_SRC | SB_1_ CLK_SRC | SB_0_ CLK_SRC |
| | FB + 0x10 | CLK_BUS3 | CLK_BUS2 | *Reserved* | *Reserved* |
| | FB + 0x14 | CLK_BUS7 | CLK_BUS6 | CLK_BUS5 | CLK_BUS4 |

### 6.8.2 CLK_SEL (READ/CLEAR)

Select if the system clock is using the local clock or the SyncBus clock. If the SyncBus PLL loses its lock, this register will revert back to the local clock.

B0: Select main clock input, 0 = local clock, 1 = SyncBus clock.

### 6.8.3 PLL_LOCKED (READ ONLY)

This register indicates when the SyncBus PLL is locked, which means that the input SyncBus clock is valid, and may be used.

B0: SyncBus PLL locked, 0 = not locked, 1 = locked.

### 6.8.4 TERM_ENABLE (READ/WRITE)

Selects if termination is enable on the SyncBus. When using the SyncBus the first and last module in the SyncBus needs to have termination enabled.

B0: Enable SyncBus termination, 0 = disabled, 1 = enabled.

### 6.8.5 ENABLE (READ/WRITE)

Select if the SyncBus driver is enable. When the SyncBus driver is disabled, the transceiver is powered down and SyncBus will not receive or transmit. This bit must be enabled in order to use the SyncBus.

B0: Enable SyncBus driver, 0 = disabled (low power), 1 = enabled.

### 6.8.6 SB_N_CLK_SRC (READ/WRITE)

Select source for SYNCBUS_N line output.

Below is the list of clock sources and the register value needed to select the source.

B[7:0]:

- 0x00: System clock/immediate
- 0x01: Never
- 0x02: CLK_BUS2
- 0x03: CLK_BUS3
- 0x04: CLK_BUS4
- 0x05: CLK_BUS5
- 0x06: CLK_BUS6
- 0x07: CLK_BUS7
- 0x08: N/A
- 0x09: N/A
- 0x0A: CLK_BUS2 Inverted
- 0x0B: CLK_BUS3 Inverted
- 0x0C: CLK_BUS4 Inverted
- 0x0D: CLK_BUS5 Inverted
- 0x0E: CLK_BUS6 Inverted
- 0x0F: CLK_BUS7 Inverted

### 6.8.7 DIRECTION (READ/WRITE)

Selects the direction of SYNCBUS_N.

***NOTE: When synchronizing multiple boards, enabling multiple outputs on a SyncBus line may result in expected errors.***

B0: Selects the direction SYNCBUS_0 line, 0 =Input, 1 = Output.

B1: Selects the direction SYNCBUS_1 line, 0 =Input, 1 = Output.

B2: Selects the direction SYNCBUS_2 line, 0 =Input, 1 = Output.

B3: Selects the direction SYNCBUS_3 (CLK) line, 0 =Input, 1 = Output.

### 6.8.8 CLK_BUSN

Selects the source to drive onto Clock Bus signal N. Values are:

B[7:0] Clock Source Select

- 0x00: Disable Clock Source
- 0x80: CLK_EVENT_SYNCBUS_0
- 0x81: CLK_EVENT_SYNCBUS_1
- 0x82: CLK_EVENT_SYNCBUS_2

# 7 Troubleshooting

If you are having problems with your system, please try the following initial steps:

- **Simplify the System** – Remove modules one at a time from your system to see if there is a specific module that is causing a problem. Perform you troubleshooting with the least number of modules in the system possible.

- **Swap Components** – Try replacing parts in the system one at a time with similar parts to determine if a part is faulty or if a type of part is configured incorrectly.

If problems persist, or you have questions about configuring this product, contact RTD Embedded Technologies via the following methods:

Phone: +1-814-234-8087
E-Mail: techsupport@rtd.com

Be sure to check the RTD web site (http://www.rtd.com) frequently for product updates, including newer versions of the board manual and application software.

# 8 Additional Information

## 8.1 PC/104 Specifications

A copy of the latest PC/104 specifications can be found on the webpage for the PC/104 Embedded Consortium:

www.pc104.org

## 8.2 PCI and PCI Express Specification

A copy of the latest PCI and PCI Express specifications can be found on the webpage for the PCI Special Interest Group:

www.pcisig.com

# 9 Limited Warranty

RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD Embedded Technologies, Inc. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, RTD Embedded Technologies will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to RTD Embedded Technologies. All replaced parts and products become the property of RTD Embedded Technologies. Before returning any product for repair, customers are required to contact the factory for a Return Material Authorization (RMA) number.

This limited warranty does not extend to any products which have been damaged as a result of accident, misuse, abuse (such as: use of incorrect input voltages, improper or insufficient ventilation, failure to follow the operating instructions that are provided by RTD Embedded Technologies, “acts of God” or other contingencies beyond the control of RTD Embedded Technologies), or as a result of service or modification by anyone other than RTD Embedded Technologies. Except as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranties of merchantability and fitness for a particular purpose, and RTD Embedded Technologies expressly disclaims all warranties not stated herein. All implied warranties, including implied warranties for merchantability and fitness for a particular purpose, are limited to the duration of this warranty. In the event the product is not free from defects as warranted above, the purchaser's sole remedy shall be repair or replacement as provided above. Under no circumstances will RTD Embedded Technologies be liable to the purchaser or any user for any damages, including any incidental or consequential damages, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

Some states do not allow the exclusion or limitation of incidental or consequential damages for consumer products, and some states do not allow limitations on how long an implied warranty lasts, so the above limitations or exclusions may not apply to you.

This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

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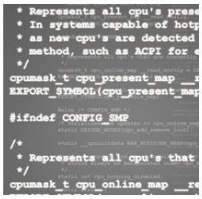

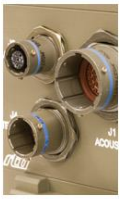
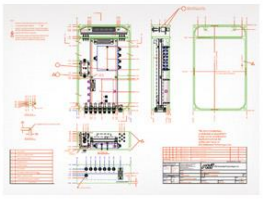

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