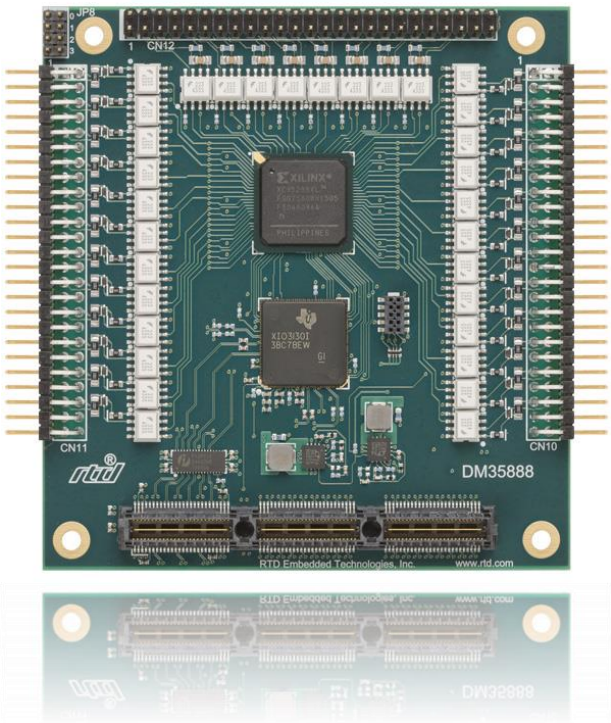
DM35888HR

PCIe/104 64-Channel High Density Isolated Digital I/O

User's Manual

BDM-610010049 Rev. F



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Revision History

Rev A	Initial Release
Rev B	Corrected Subsystem Vendor and Subsystem ID in Table 10 on page 21. Corrected pin numbers in Table 5 on page 11. Corrected title of Table 6 on page 12.
Rev C	Added ASPM note. Changed to 0 based numbering. Corrected maximum and minimum input voltage specification. Added 24V version. Added MTBF.
Rev D	Added IDAN connections.
Rev E	Corrected connector pin numbering in Table 6. Added User ID Jumpers.
Rev F	Corrected User ID jumper description in Section 3.3.3.

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1 Introduction

1.1 Product Overview

The DM35888HR provides Opto-Isolated Digital Inputs and Outputs to interface with a variety of devices. The Inputs allow for a broad range of input voltages, and are compatible with 5V systems and 120V systems. The high-current Outputs allow for driving LEDs, relays, and solenoids. The PCIe interface provides compatibility with the latest generation of CPUs, and the PCIe lane repopulation allows for virtually limitless system expansion.

1.2 Board Features

- PC/104 form factor
- PCIe/104 stackable bus structure
  - PCIe/104 Universal Connector
  - PCI Express (PCIe) x1 Upstream Interface to CPU
  - Uses a PCIe x1 link
  - Repopulates the PCIe bus
- Broad input voltage range
- High-current outputs
- -40 to +85°C Operation
- Isolated Input
  - 48 Opto-Isolated digital Inputs
  - Two 50 position 0.1" DIL headers
  - Maximum Input Voltage:
    - Standard Version: $15V_{DC}$
    - 24V Version: $30V_{DC}$
  - Reverse-polarity protection
  - 2500 $V_{AC(RMS)}$ Isolation
  - Custom settings available
- Isolated Output
  - 16 Opto-Isolated digital outputs
  - One 50 position 0.1" DIL header
  - Open-Collector outputs
  - 4.75k Ohm Pull-Up resistor
  - Maximum Output Current: 100mA at 55 C, 50mA at 85C
  - Maximum Output Voltage: 30V
  - 2500 $V_{AC(RMS)}$ Isolation

1.3 Ordering Information

The DM35888HR is available with the following options:

Table 1: Ordering Options

Part Number	Description
DM35888HR	PCIe/104 64-Channel High Density Isolated Digital I/O Module for 5V and 12V systems
DM35888HR-24V	PCIe/104 64-Channel High Density Isolated Digital I/O Module for 24V systems
IDAN-DM35888HR-D	PCIe/104 64-Channel High Density Isolated Digital I/O Module in IDAN enclosure
IDAN-DM35888HR-24V-D	PCIe/104 64-Channel High Density Isolated Digital I/O Module in IDAN enclosure for 24V systems

The Intelligent Data Acquisition Node (IDAN®) building block can be used in just about any combination with other IDAN building blocks to create a simple but rugged 104™ stack. This module can also be incorporated in a custom-built RTD HiDAN™ or HiDANplus High Reliability Intelligent Data Acquisition Node. Contact RTD sales for more information on our high reliability systems.

1.4 Contact Information

1.4.1 Sales Support

For sales inquiries, you can contact RTD Embedded Technologies sales via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: sales@rtd.com

1.4.2 Technical Support

If you are having problems with you system, please try the steps in the Troubleshooting section of this manual on page 21.

For help with this product, or any other product made by RTD, you can contact RTD Embedded Technologies technical support via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: techsupport@rtd.com

2 Specifications

2.1 Operating Conditions

Table 2: Operating Conditions

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{cc5}	5V Supply Voltage		4.75	5.25	V
V_{cc3}	3.3V Supply Voltage		n/a	n/a	V
V_{cc12}	12V Supply Voltage		n/a	n/a	V
V_{cc-12}	-12V Supply Voltage		n/a	n/a	V
T_a	Operating Temperature		-40	+85	C
T_s	Storage Temperature		-55	+125	C
RH	Relative Humidity	Non-Condensing	0	90%	%
MTBF	Mean Time Before Failure	Telcordia Issue 2 30°C, Ground benign, controlled		1,909,967	Hours

2.2 Electrical Characteristics

Table 3: Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
P	Power Consumption	V_{cc5} = 5.0V		2.5	W
I_{cc5}	5V Input Supply Current	Active		500	mA
		PCIe Bus			
	Differential Output Voltage		0.8	1.2	V
	DC Differential TX Impedance		95.2	116.9	Ω
	Differential Input Voltage		0.175	3.3	V
	DC Differential RX Impedance		92.7	115.8	Ω
	Electrical Idle Detect Threshold		61	173	mV
		Isolated Inputs			
	Input Voltage	Standard Version 24V	-15 -30	15 30	V_{DC}
	Turn-On Threshold Voltage	Standard Version 24V	1.0 1.0	2.4 4.5	V_{DC}
	Turn-On Threshold Current			500	µA
	Isolation Voltage			2500	$V_{AC(RMS)}$
		Isolated Outputs			
	Bias Voltage		0	30	V_{DC}
	Output Current	T_a = 55C		100	mA
	Output Current	T_a = 85C		50	mA
	Isolation Voltage			2500	$V_{AC(RMS)}$

3 Board Connection

NOTE: It may be necessary to disable PCIe Active State Power Management (ASPM) in the BIOS setup utility for correct operation. This is typically in the "Advanced/PCI Express/Port #" menu. Contact your CPU vendor for details.

3.1 Board Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your board in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the board at the edges, and do not touch the components or connectors. Handle the board in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

3.2 Physical Characteristics

STEP model is available upon request; contact RTD Tech Support for more information.

- Weight: Approximately 0.16 lbs. (72 g)
- Dimensions: 90.17 mm L x 95.89 mm W (3.550 in L x 3.775 in W)
- Stand-off Height: 0.600 inches (15.240 mm)

3.3 Connectors and Jumpers

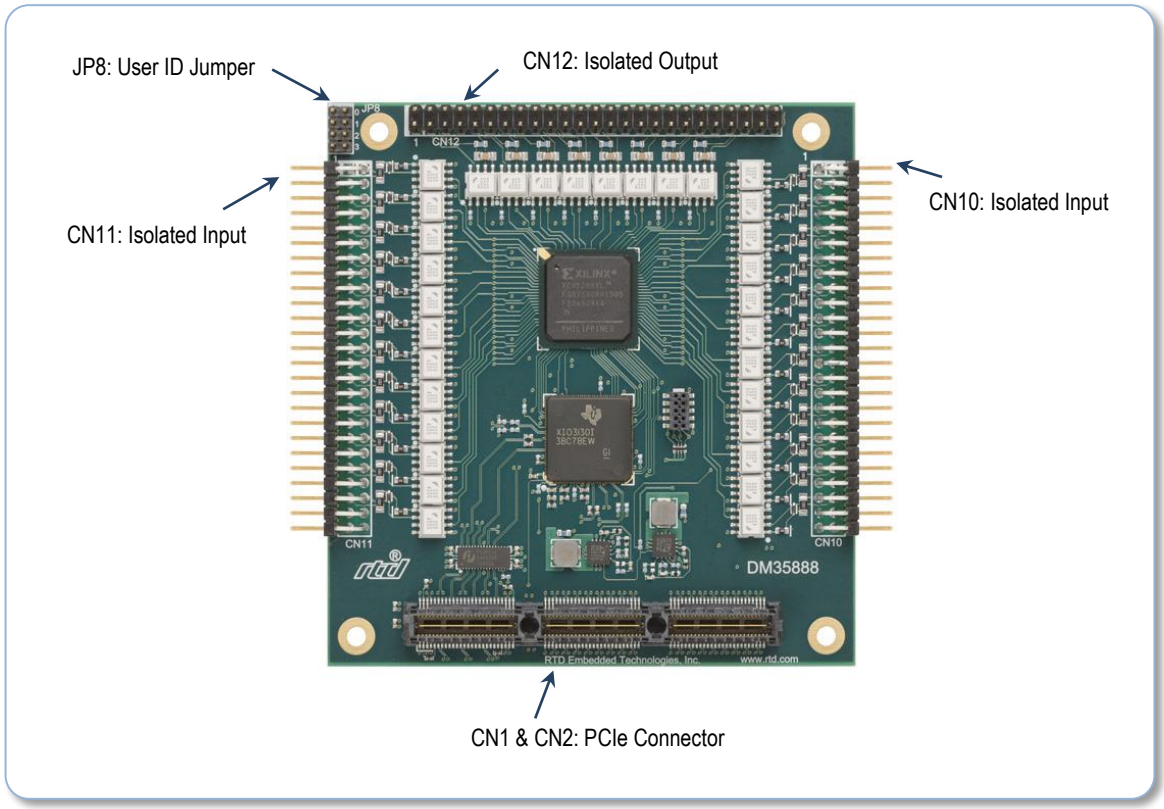

Figure 1: Board Connections

3.3.1 EXTERNAL I/O CONNECTORS

CN10 and CN11: Isolated Input

Connector Part #: SAMTEC TSW-125-08-S-D-RA **Mating Connector:** FCI 65043-012 LF

The Isolated Inputs are on CN10 and CN11. The pin assignments are shown in the Table below. The Figure below shows the input circuit.

Table 4: CN10 Isolated Input

Pin Name	#	#	Pin Name
IN0-	2	1	IN0+
IN1-	4	3	IN1+
IN2-	6	5	IN2+
IN3-	8	7	IN3+
IN4-	10	9	IN4+
IN5-	12	11	IN5+
IN6-	14	13	IN6+
IN7-	16	15	IN7+
IN8-	18	17	IN8+
IN9-	20	19	IN9+
IN10-	22	21	IN10+
IN11-	24	23	IN11+
IN12-	26	25	IN12+
IN13-	28	27	IN13+
IN14-	30	29	IN14+
IN15-	32	31	IN15+
IN16-	34	33	IN16+
IN17-	36	35	IN17+
IN18-	38	37	IN18+
IN19-	40	39	IN19+
IN20-	42	41	IN20+
IN21-	44	43	IN21+
IN22-	46	45	IN22+
IN23-	48	47	IN23+
n.c.	50	49	n.c.

Table 5: CN11 Isolated Input

Pin Name	#	#	Pin Name
IN24-	2	1	IN24+
IN25-	4	3	IN25+
IN26-	6	5	IN26+
IN27-	8	7	IN27+
IN28-	10	9	IN28+
IN29-	12	11	IN29+
IN30-	14	13	IN30+
IN31-	16	15	IN31+
IN32-	18	17	IN32+
IN33-	20	19	IN33+
IN34-	22	21	IN34+
IN35-	24	23	IN35+
IN36-	26	25	IN36+
IN37-	28	27	IN37+
IN38-	30	29	IN38+
IN39-	32	31	IN39+
IN40-	34	33	IN40+
IN41-	36	35	IN41+
IN42-	38	37	IN42+
IN43-	40	39	IN43+
IN44-	42	41	IN44+
IN45-	44	43	IN45+
IN46-	46	45	IN46+
IN47-	48	47	IN47+
n.c.	50	49	n.c.

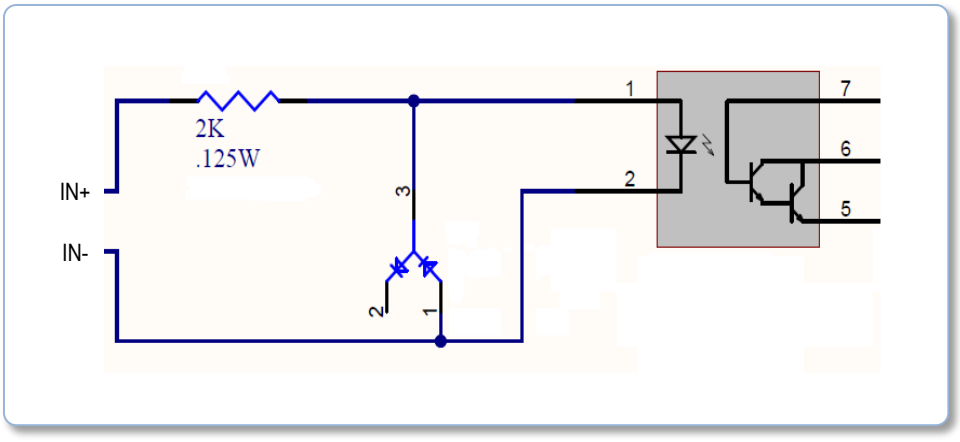

Figure 2: Isolated Input Circuit

CN12: Isolated Output

Connector Part #: SAMTEC TSW-125-16-S-D **Mating Connector:** FCI 65043-012 LF

The Isolated Outputs are on CN12. The pin assignments are shown in the Table below. The Figure below shows the input circuit.

Table 6: CN12 Isolated Output

Pin Name	#	#	Pin Name
Out0	2	1	+Vsupply-0
+Vsupply-1	4	3	GND-0
GND-1	6	5	Out1
Out2	8	7	+Vsupply-2
+Vsupply-3	10	9	GND-2
GND-3	12	11	Out3
Out4	14	13	+Vsupply-4
+Vsupply-5	16	15	GND-4
GND-5	18	17	Out5
Out6	20	19	+Vsupply-6
+Vsupply-7	22	21	GND-6
GND-7	24	23	Out7
Out8	26	25	+Vsupply-8
+Vsupply-9	28	27	GND-8
GND-9	30	29	Out9
Out10	32	31	+Vsupply-10
+Vsupply-11	34	33	GND-10
GND-11	36	35	Out11
Out12	38	37	+Vsupply-12
+Vsupply-13	40	39	GND-12
GND-13	42	41	Out13
Out14	44	43	+Vsupply-14
+Vsupply-15	46	45	GND-14
GND-15	48	47	Out15
n.c.	50	49	n.c.

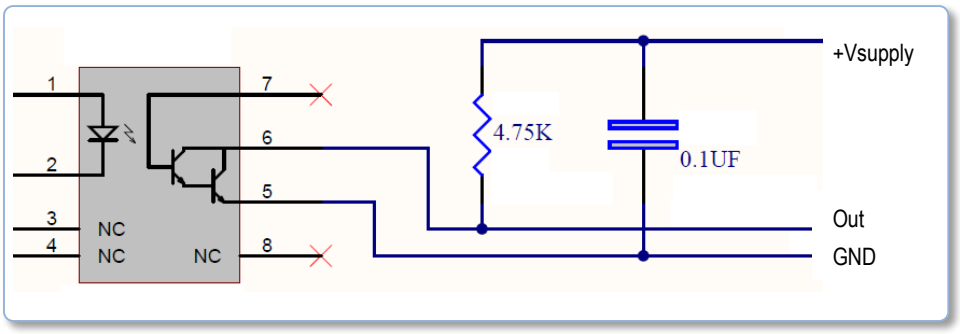

Figure 3: Isolated Output Circuit

3.3.2 BUS CONNECTORS

CN1 (Top) & CN2 (Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 27)

The DM35888HR is a "Universal" board, and can connect to either a Type 1 or Type 2 PCIe/104 connector.

3.3.3 JUMPERS

User ID Jumper

The User ID Jumper is a four position, user defined jumper block. It can be used to uniquely identify multiple boards in the system. The jumper settings can be read from the USER_ID register. An installed jumper results in a logic high, and an open jumper results in a logic low.

Table 7: JP8 – User ID Jumper

Position	Description
1-2	User ID bit 0
3-4	User ID bit 1
5-6	User ID bit 2
7-8	User ID bit 3

3.4 Steps for Installing

NOTE: It may be necessary to disable PCIe Active State Power Management (ASPM) in the BIOS setup utility for correct operation. This is typically in the "Advanced/PCI Express/Port #" menu. Contact your CPU vendor for details.

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the PC/104 system or stack.
3. Select and install stand-offs to properly position the module on the stack.
4. Remove the module from its anti-static bag.
5. Check that pins of the bus connector are properly positioned.
6. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
7. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
8. Gently and evenly press the module onto the PC/104 stack.
9. If any boards are to be stacked above this module, install them.
10. Attach any necessary cables to the PC/104 stack.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

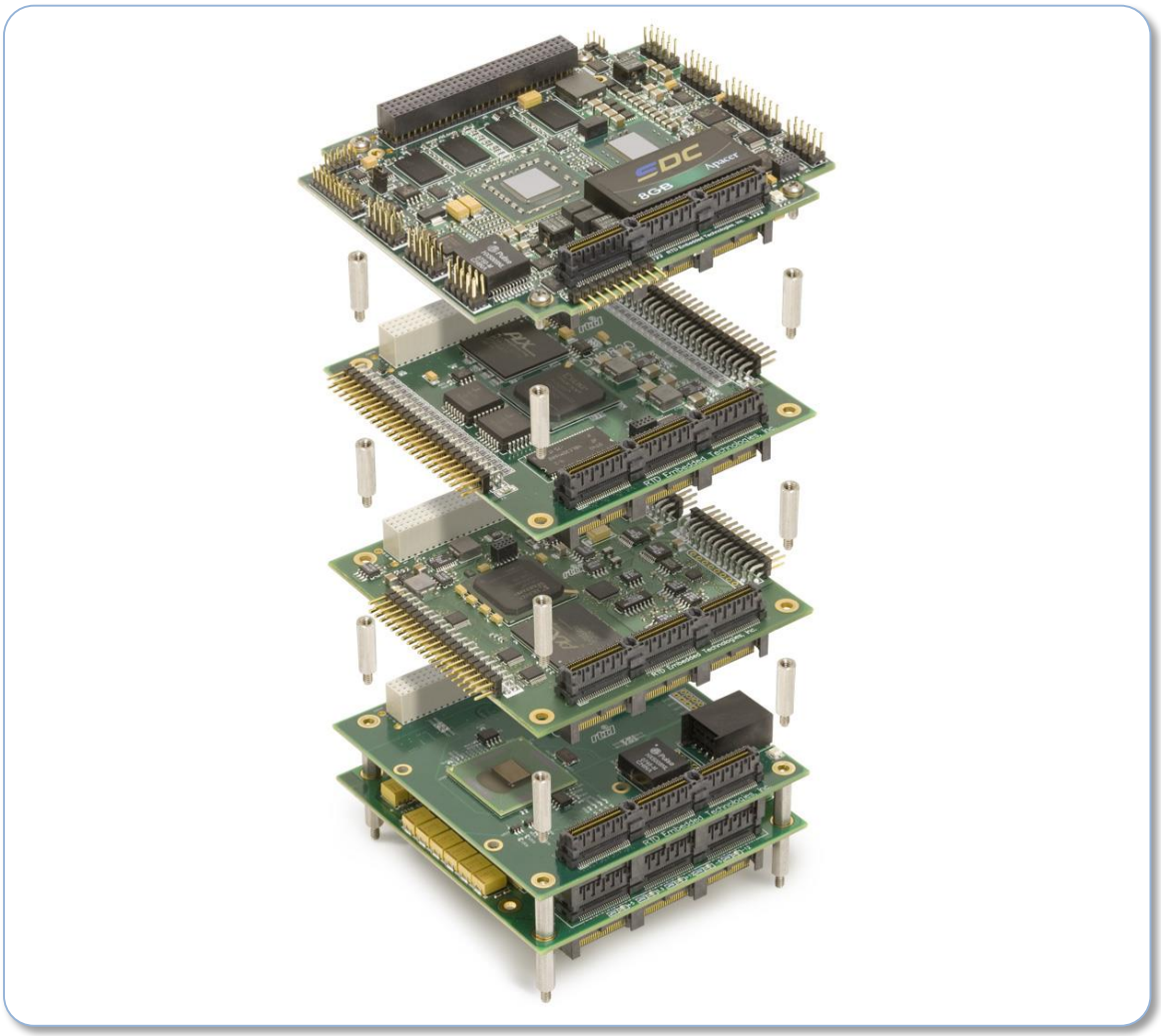

Figure 4: Example 104™ Stack

4 IDAN Connections

4.1 Module Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your module in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the module by the aluminum enclosure, and do not touch the components or connectors. Handle the module in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

4.2 Physical Characteristics

- Weight: Approximately 0.42 Kg (0.92 lbs.)
- Dimensions: 152mm L x 130mm W x 34mm H (5.983" L x 5.117" W x 1.339" H)

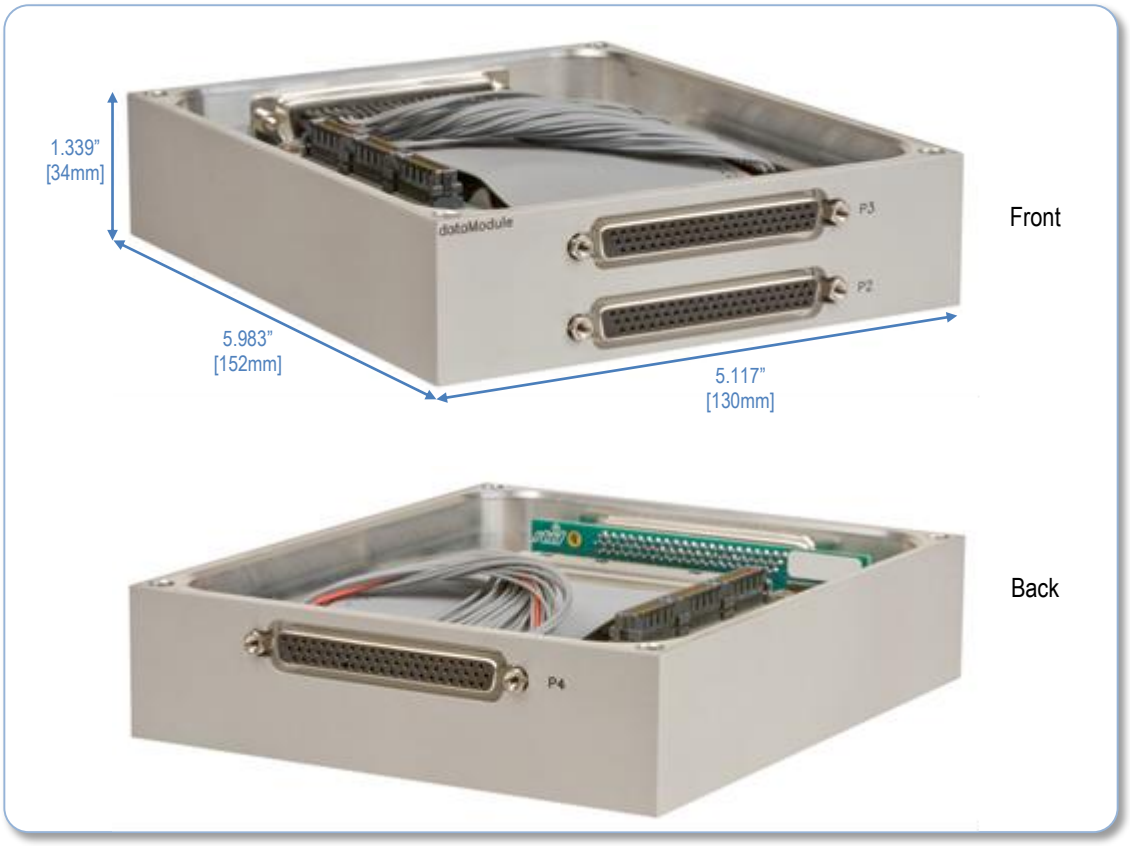

Figure 5: IDAN Dimensions

4.3 Connectors

4.3.1 External I/O Connectors

P2 & P3: Isolated Input Connector

Connector Part #: VALCONN HDB-62S **Mating Connector:** VALCONN HDB-62P

The Isolated Inputs are on P2 and P3, which are connected to CN10 and CN11 respectively. The pin assignments are shown in the Table below.

Table 8: P2 and P3 Pin Assignments

IDAN P2 Pin				CN10
Row 1	Row 2	Row 3	Signal	Pin
1			IN0+	1
	22		IN0-	2
		43	IN1+	3
2			IN1-	4
	23		IN2+	5
		44	IN2-	6
3			IN3+	7
	24		IN3-	8
		45	IN4+	9
4			IN4-	10
	25		IN5+	11
		46	IN5-	12
5			IN6+	13
	26		IN6-	14
		47	IN7+	15
6			IN7-	16
	27		IN8+	17
		48	IN8-	18
7			IN9+	19
	28		IN9-	20
		49	IN10+	21
8			IN10-	22
	29		IN11+	23
		50	IN11-	24
9			IN12+	25
	30		IN12-	26
		51	IN13+	27
10			IN13-	28
	31		IN14+	29
		52	IN14-	30
11			IN15+	31
	32		IN15-	32
		53	IN16+	33
12			IN16-	34
	33		IN17+	35
		54	IN17-	36
13			IN18+	37
	34		IN18-	38
		55	IN19+	39
14			IN19-	40
	35		IN20+	41
		56	IN20-	42
15			IN21+	43
	36		IN21-	44
		57	IN22+	45
16			IN22-	46
	37		IN23+	47

IDAN P3 Pin				CN11
Row 1	Row 2	Row 3	Signal	Pin
1			IN24+	1
	22		IN24-	2
		43	IN25+	3
2			IN25-	4
	23		IN26+	5
		44	IN26-	6
3			IN27+	7
	24		IN27-	8
		45	IN28+	9
4			IN28-	10
	25		IN29+	11
		46	IN29-	12
5			IN30+	13
	26		IN30-	14
		47	IN31+	15
6			IN31-	16
	27		IN32+	17
		48	IN32-	18
7			IN33+	19
	28		IN33-	20
		49	IN34+	21
8			IN34-	22
	29		IN35+	23
		50	IN35-	24
9			IN36+	25
	30		IN36-	26
		51	IN37+	27
10			IN37-	28
	31		IN38+	29
		52	IN38-	30
11			IN39+	31
	32		IN39-	32
		53	IN40+	33
12			IN40-	34
	33		IN41+	35
		54	IN41-	36
13			IN42+	37
	34		IN42-	38
		55	IN43+	39
14			IN43-	40
	35		IN44+	41
		56	IN44-	42
15			IN45+	43
	36		IN45-	44
		57	IN46+	45
16			IN46-	46
	37		IN47+	47

Table 8: P2 and P3 Pin Assignments

IDAN P2 Pin			Signal	CN10 Pin
Row 1	Row 2	Row 3		
		58	IN23-	48
17			*Reserved*	49
	38		*Reserved*	50
		59	*Reserved*	
18			*Reserved*	
	39		*Reserved*	
		60	*Reserved*	
19			*Reserved*	
	40		*Reserved*	
		61	*Reserved*	
20			*Reserved*	
	41		*Reserved*	
		62	*Reserved*	
21			*Reserved*	
	42		*Reserved*	

IDAN P3 Pin			Signal	CN11 Pin
Row 1	Row 2	Row 3		
		58	IN47-	48
17			*Reserved*	49
	38		*Reserved*	50
		59	*Reserved*	
18			*Reserved*	
	39		*Reserved*	
		60	*Reserved*	
19			*Reserved*	
	40		*Reserved*	
		61	*Reserved*	
20			*Reserved*	
	41		*Reserved*	
		62	*Reserved*	
21			*Reserved*	
	42		*Reserved*	

P4: Isolated Output Connector

Connector Part #: VALCONN HDB-62S **Mating Connector:** VALCONN HDB-62P

The Isolated Outputs are on P4, which is connected to CN12. The pin assignments are shown in the Table below.

Table 9: P4 Pin Assignments

IDAN P4 Pin			Signal	C12 Pin
Row 1	Row 2	Row 3		
1			+Vsupply-0	1
	22		Out0	2
		43	GND-0	3
2			+Vsupply-1	4
	23		Out1	5
		44	GND-1	6
3			+Vsupply-2	7
	24		Out2	8
		45	GND-2	9
4			+Vsupply-3	10
	25		Out3	11
		46	GND-3	12
5			+Vsupply-4	13
	26		Out4	14
		47	GND-4	15
6			+Vsupply-5	16
	27		Out5	17
		48	GND-5	18
7			+Vsupply-6	19
	28		Out6	20
		49	GND-6	21
8			+Vsupply-7	22
	29		Out7	23
		50	GND-7	24
9			+Vsupply-8	25
	30		Out8	26
		51	GND-8	27
10			+Vsupply-9	28
	31		Out9	29
		52	GND-9	30
11			+Vsupply-10	31
	32		Out10	32

Table 9: P4 Pin Assignments

IDAN P4 Pin				C12
Row 1	Row 2	Row 3	Signal	Pin
		53	GND-10	33
12			+Vsupply-11	34
	33		Out11	35
		54	GND-11	36
13			+Vsupply-12	37
	34		Out12	38
		55	GND-12	39
14			+Vsupply-13	40
	35		Out13	41
		56	GND-13	42
15			+Vsupply-14	43
	36		Out14	44
		57	GND-14	45
16			+Vsupply-15	46
	37		Out15	47
		58	GND-15	48
17			*Reserved*	49
	38		*Reserved*	50
		59	*Reserved*	
18			*Reserved*	
	39		*Reserved*	
		60	*Reserved*	
19			*Reserved*	
	40		*Reserved*	
		61	*Reserved*	
20			*Reserved*	
	41		*Reserved*	
		62	*Reserved*	
21			*Reserved*	
	42		*Reserved*	

4.3.2 BUS CONNECTORS

CN1 (Top) & CN2 (Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 27)

The DM35888HR is a "Universal" board, and can connect to either a Type 1 or Type 2 PCIe/104 connector.

4.4 Steps for Installing

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the IDAN system.
3. Remove the module from its anti-static bag.
4. Check that pins of the bus connector are properly positioned.
5. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
6. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
7. Gently and evenly press the module onto the IDAN system.
8. If any boards are to be stacked above this module, install them.
9. Finish assembling the IDAN stack by installing screws of an appropriate length.
10. Attach any necessary cables to the IDAN system.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

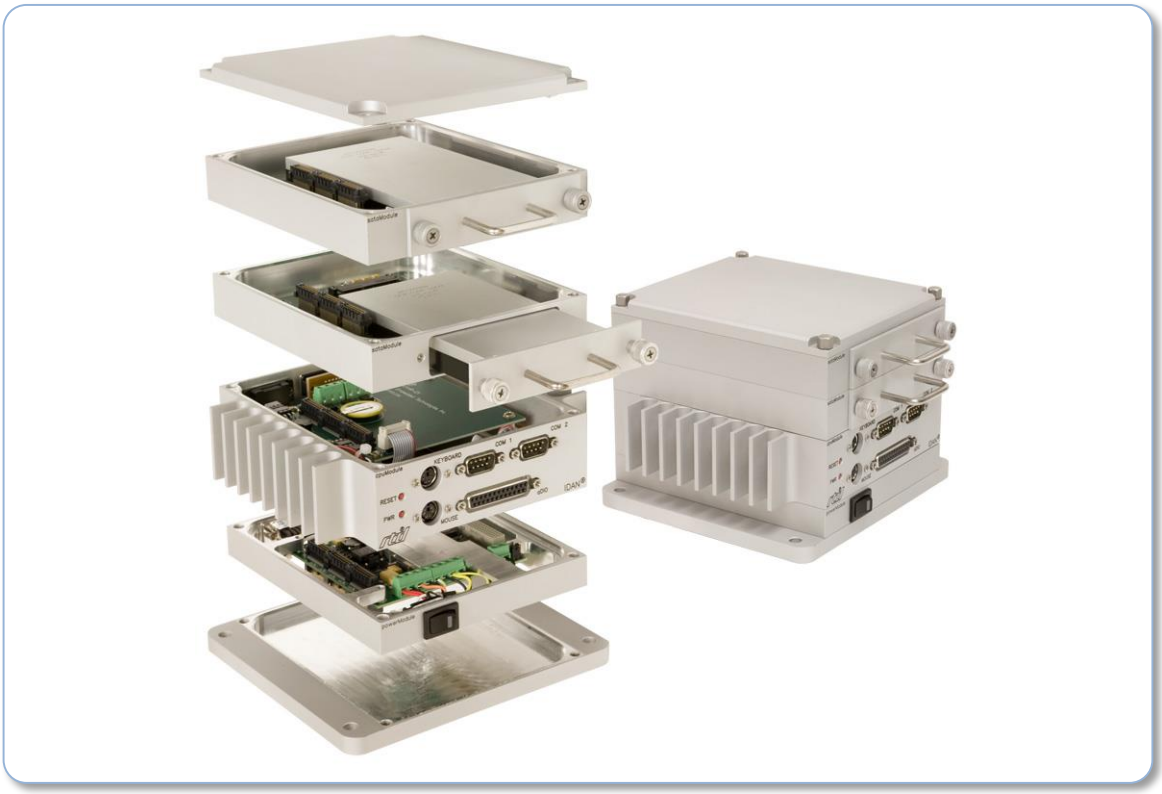

Figure 6: Example IDAN System

5 Functional Description

5.1 Block Diagram

The Figure below shows the functional block diagram of the DM35888HR. The various parts of the block diagram are discussed in the following sections.

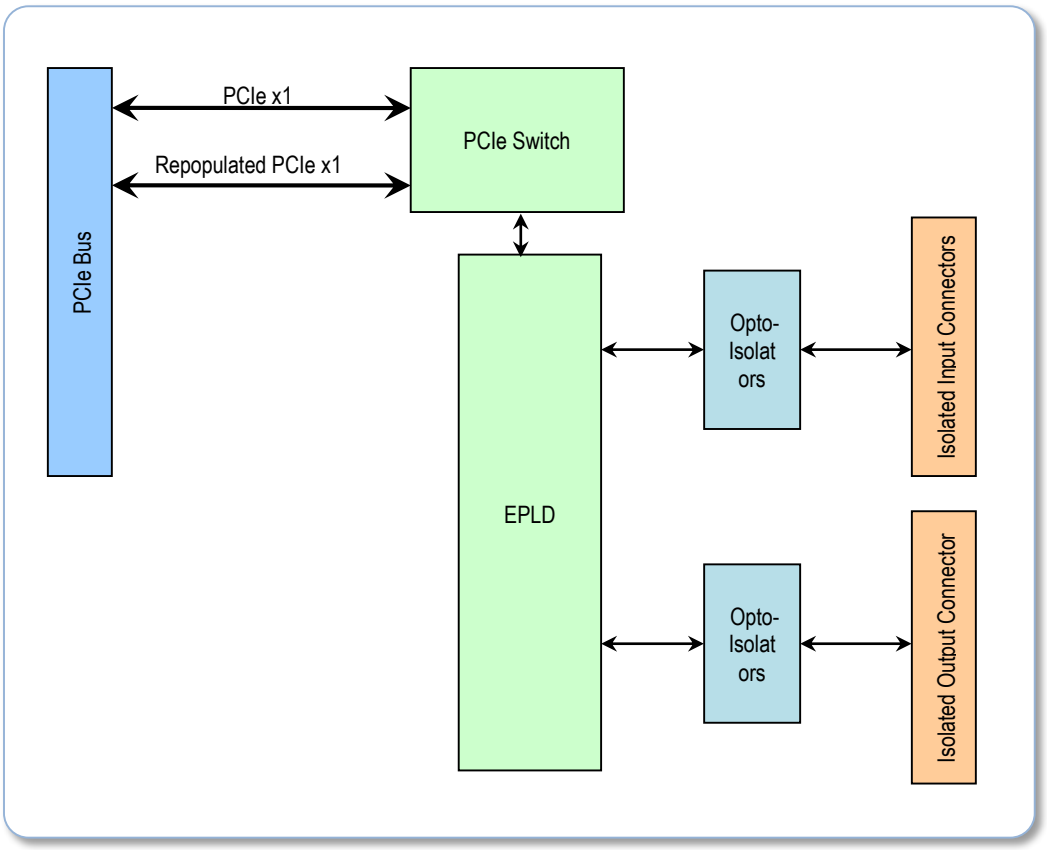

Figure 7: DM35888HR Block Diagram

5.2 PCIe Switch

The PCI Express Switch provides the bus interface to the DM35888HR. The switch includes GPIO that are accessible from its Configuration Space, which is configured as a generic bus. This is a low speed interface that does not provide support for interrupts or DMA.

The PCIe Switch also provides lane repopulation. One lane is used as the uplink to the CPU. On the opposite side of the board it is replaced by a lane from the switch. This allows a virtually limitless number of boards to be added to the system.

5.3 EPLD

The EPLD provides glue logic between the PCIe interface and the on-board functions.

5.4 Opto-Isolators

The opto-isolators provide the isolation and input/output circuit for the digital I/O.

6 Register Address Space

The bus interface is provided through the GPIO of the PCIe Switch. The GPIO are configured as a generic bus, and the board registers are accessed through an index and data register. The following sections describe the steps needed to access the board registers.

NOTE: It may be necessary to disable PCIe Active State Power Management (ASPM) in the BIOS setup utility for correct operation. This is typically in the "Advanced/PCI Express/Port #" menu. Contact your CPU vendor for details.

6.1 Identifying the Board

The DM35888HR shows up in standard PCI Configuration space as a set of PCI to PCI Bridges. It can be positively identified as shown in the Table below.

Table 10: Identifying the DM35888HR

Configuration Space Offset	Register Description	Value
0x00	Vendor ID	0x104C
0x02	Device ID	0x8232
0x84	Subsystem Vendor ID	0x1435
0x86	Subsystem ID	0x5888

6.2 Index and Data Registers

Table 11: Index and Data Registers

Configuration Space Offset	0x03	0x02	0x01	0x00
0xBC	GPIOAB_CTRL			
0xC0	GPIOCD_CTRL			
0xC4	SELECT		INDEX_DATA	

6.2.1 GPIOAB_CTRL (READ/WRITE)

This register is used to set the direction for the GPIO port. The values to write to it are:

0x12491249 for a Write operation
0x00000000 for a Read operation

6.2.2 GPIOCD_CTRL (READ/WRITE)

This register is used to set the direction for the GPIO port. The values to write to it are:

0x01491249 for a Write operation
0x01480000 for a Read operation

6.2.3 SELECT (READ/WRITE)

This register is used to select between the Index and Data register. All undefined bits may be written with a 0.

B2: DATA
0 = Accessing Index register
1 = Accessing Data register
B1:WR_STRB
Writes take effect on 0 to 1 transition

B0: OE#

0 = Output of EPLD is enabled (for reads)
1 = Output of EPLD is disabled (for writes)

6.2.4 INDEX_DATA (READ/WRITE)

This register is used to access the Index or Data register.

NOTE: The SELECT and INDEX_DATA register may be accessed using a single 32-bit operation.

6.3 Accessing the Board Registers

6.3.1 READING FROM A BOARD REGISTER

To read one of the Board Registers, use the following steps:

1. Read the GPIOAB_CTRL, GPIOCD_CTRL, SELECT and INDEX_DATA registers and store them so they can be restored.
2. Save the Index Register
    a. Set GPIOAB_CTRL and GPIOCD_CTRL to their Read values.
    b. Set SELECT such that DATA=0, WR_STRB=0, and OE#=0
    c. Read INDEX_DATA and store it as the Old Index.
3. Set the Index Register
    a. Set SELECT such that DATA=0, WR_STRB=0, and OE#=1 and set INDEX_DATA to the desired Index.
    b. Set GPIOAB_CTRL and GPIOCD_CTRL to their Write values.
    c. Set SELECT such that DATA=0, WR_STRB=1, and OE#=1. (May also set INDEX_DATA to the desired Index again).
4. Read the Data Register
    a. Set GPIOAB_CTRL and GPIOCD_CTRL to their Read values.
    b. Set SELECT such that DATA=1, WR_STRB=0, and OE#=0
    c. Read INDEX_DATA as the desired Data.
5. Restore the Index Register
    a. Set SELECT such that DATA=0, WR_STRB=0, and OE#=1 and set INDEX_DATA to the Old Index.
    b. Set GPIOAB_CTRL and GPIOCD_CTRL to their Write values.
    c. Set SELECT such that DATA=0, WR_STRB=1, and OE#=1. (May also set INDEX_DATA to the Old Index again).
6. Restore Other Registers
    a. Restore GPIOAB_CTRL
    b. Restore GPIOCD_CTRL bit-wise or'ed with the Read Value (to make sure the SELECT pins are always output)
    c. Restore SELECT and INDEX_DATA with the WR_STRB bit cleared (to make sure a write isn't duplicated)

NOTE: If multi-thread safe operation is not required, steps 1, 2, 5, and 6 can be eliminated.

6.3.2 WRITING TO A BOARD REGISTER

To write to one of the Board Registers, use the following steps:

1. Read the GPIOAB_CTRL, GPIOCD_CTRL, SELECT and INDEX_DATA registers and store them so they can be restored.
2. Save the Index Register
    a. Set GPIOAB_CTRL and GPIOCD_CTRL to their Read values.
    b. Set SELECT such that DATA=0, WR_STRB=0, and OE#=0
    c. Read INDEX_DATA and store it as the Old Index.
3. Set the Index Register
    a. Set SELECT such that DATA=0, WR_STRB=0, and OE#=1 and set INDEX_DATA to the desired Index.
    b. Set GPIOAB_CTRL and GPIOCD_CTRL to their Write values.
    c. Set SELECT such that DATA=0, WR_STRB=1, and OE#=1. (May also set INDEX_DATA to the desired Index again).
4. Set the Data Register
    a. Set SELECT such that DATA=1, WR_STRB=0, and OE#=1 and set INDEX_DATA to the desired Data.
    b. Set GPIOAB_CTRL and GPIOCD_CTRL to their Write values. (Already set by Step 3 above)
    c. Set SELECT such that DATA=1, WR_STRB=1, and OE#=1. (May also set INDEX_DATA to the desired Data again).
5. Restore the Index Register
    a. Set SELECT such that DATA=0, WR_STRB=0, and OE#=1 and set INDEX_DATA to the Old Index.
    b. Set GPIOAB_CTRL and GPIOCD_CTRL to their Write values. (Already set by Step 3 above)
    c. Set SELECT such that DATA=0, WR_STRB=1, and OE#=1. (May also set INDEX_DATA to the Old Index again).
6. Restore Other Registers
    a. Restore GPIOAB_CTRL
    b. Restore GPIOCD_CTRL bit-wise or'ed with the Read Value (to make sure the SELECT pins are always output)
    c. Restore SELECT and INDEX_DATA with the WR_STRB bit cleared (to make sure a write isn't duplicated)

NOTE: If multi-thread safe operation is not required, steps 1, 2, 5, and 6 can be eliminated.

6.3.3 READING SHIFT REGISTER STATUS

The Index Register includes a Read-Only bit indicating whether the shift register is busy. This can be accessed as follows:

1. Read the GPIOAB_CTRL, GPIOCD_CTRL, SELECT and INDEX_DATA registers and store them so they can be restored.
2. Read the Index/Status Register
    a. Set GPIOAB_CTRL and GPIOCD_CTRL to their Read values.
    b. Set SELECT such that DATA=0, WR_STRB=0, and OE#=0
    c. Read INDEX_DATA. Bit 8 is set if the Shift Register is busy, and cleared if the Shift Register is idle.
3. Restore Other Registers
    a. Restore GPIOAB_CTRL
    b. Restore GPIOCD_CTRL bit-wise or'ed with the Read Value (to make sure the SELECT pins are always output)
    c. Restore SELECT and INDEX_DATA with the WR_STRB bit cleared (to make sure a write isn't duplicated)

NOTE: If multi-thread safe operation is not required, steps 1, and 3 can be eliminated.

6.4 Board Registers

Table 12: Board Registers

Index	Data (16-bit)
0x00	BUILD_NUM_LS
0x01	BUILD_NUM_MS
0x02	USER_ID
0x03	Reserved
0x04	OPTO_IN_A
0x05	OPTO_IN_B
0x06	OPTO_IN_C
0x07	OPTO_OUT

6.4.1 BUILD_NUM_LS, BUILD_NUM_MS (READ-ONLY)

These two registers contain the build number of the EPLD. It can be used to track revisions of the EPLD. BUILD_NUM_LS is the least-significant word, and BUILD_NUM_MS is the most significant word.

6.4.2 USER_ID (READ-ONLY)

This register shows the status of the User ID Jumpers

B0: User ID 0 Jumper. 0 = Open, 1 = Closed

B1: User ID 1 Jumper. 0 = Open, 1 = Closed

B2: User ID 2 Jumper. 0 = Open, 1 = Closed

B3: User ID 3 Jumper. 0 = Open, 1 = Closed

6.4.3 OPTO_IN_A (READ-ONLY)

This register provides access to IN0 through IN15. Bit 0 corresponds to IN0, and Bit 15 corresponds to IN15. For each bit, a '0' indicates that a voltage is applied to the input, and a value of '1' indicates that there is no voltage on the input.

6.4.4 OPTO_IN_B (READ-ONLY)

This register provides access to IN16 through IN31. Bit 0 corresponds to IN16, and Bit 15 corresponds to IN31. For each bit, a '0' indicates that a voltage is applied to the input, and a value of '1' indicates that there is no voltage on the input.

6.4.5 OPTO_IN_C (READ-ONLY)

This register provides access to IN32 through IN47. Bit 0 corresponds to IN32, and Bit 15 corresponds to IN47. For each bit, a '0' indicates that a voltage is applied to the input, and a value of '1' indicates that there is no voltage on the input.

6.4.6 OPTO_OUT (READ/WRITE)

This register sets the values of the Outputs. Bit 0 corresponds to OUT0, and Bit 15 corresponds to OUT15. For each bit, a '0' causes the output is open (allowed to be pulled up by the resistor), and a value of '1' causes the output to be closed.

7 Troubleshooting

NOTE: It may be necessary to disable PCIe Active State Power Management (ASPM) in the BIOS setup utility for correct operation. This is typically in the "Advanced/PCI Express/Port #" menu. Contact your CPU vendor for details.

If you are having problems with your system, please try the following initial steps:

- **Simplify the System** – Remove modules one at a time from your system to see if there is a specific module that is causing a problem. Perform you troubleshooting with the least number of modules in the system possible.

- **Swap Components** – Try replacing parts in the system one at a time with similar parts to determine if a part is faulty or if a type of part is configured incorrectly.

If problems persist, or you have questions about configuring this product, contact RTD Embedded Technologies via the following methods:

Phone: +1-814-234-8087
E-Mail: techsupport@rtd.com

Be sure to check the RTD web site (http://www.rtd.com) frequently for product updates, including newer versions of the board manual and application software.

8 Additional Information

8.1 PC/104 Specifications

A copy of the latest PC/104 specifications can be found on the webpage for the PC/104 Embedded Consortium:

www.pc104.org

8.2 PCI and PCI Express Specification

A copy of the latest PCI and PCI Express specifications can be found on the webpage for the PCI Special Interest Group:

www.pcisig.com

9 Limited Warranty

RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD Embedded Technologies, Inc. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, RTD Embedded Technologies will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to RTD Embedded Technologies. All replaced parts and products become the property of RTD Embedded Technologies. Before returning any product for repair, customers are required to contact the factory for a Return Material Authorization (RMA) number.

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This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

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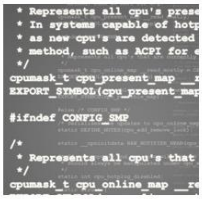

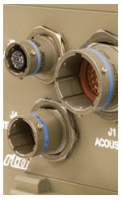
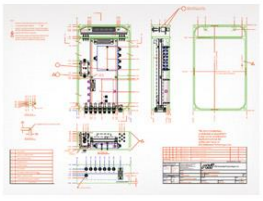

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