FPGA35S6045HR

FPGA35S6100HR

FPGA Module

User's Manual

BDM-610010045 Rev. D

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AS9100 and ISO 9001 Certified

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Revision History

Rev A	Initial Release
Rev B	Corrected pin names in Table 5 on page 13. Corrected FPGA Bank designations in CN4 & CN9: Digital I/O Connector on page 14. Added IDAN connector section.
Rev C	Change IDAN JTAG signals from P2 to P3 in Table 14 on page 18.
Rev D	Updated pictures. Changed JP7 to three-pin. Added User ID jumpers. Added embedded programmer, configuration flash, PCI vendor and device ID.
Rev E	Added ordering options for IDAN-FPGA35S6045HR-68D and IDAN-FPGA35S6100HR-68D and corresponding tables to the IDAN connector section. Corrected pin naming on IDAN 62-pin mapping for P3 pin 60 (renamed "GND_TCK" to "GND"). Add mating connectors for board level product.

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1 Introduction

1.1 Product Overview

The FPGA35S6 series of FPGA boards are designed to provide platform to create any digital I/O that is required for your application. It interfaces with the PCIe bus and features a Xilinx Spartan 6 FPGA with a 27 MHz oscillator and 1Gb of DDR2 SDRAM. There 48 5V tolerant I/O and 40 3.3V tolerant high speed I/O.

1.2 Board Features

- Xilinx Spartan 6 System level features
  - XC6SLX45T-2FGG484I
    - 43,661 Logic Cells
    - 2,489 kb of internal RAM
      - 116 18Kb (2088 Kb Max) Block RAM
      - 401 kB Distributed RAM
    - XCF16PFSG48C Configuration Flash
  - XC6SLX100T-2FGG484I
    - 101,261 Logic Cells
    - 5,800 kb of internal RAM
      - 268 18Kb (4,824 Kb Max) Block RAM
      - 976 kB Distributed RAM
    - XCF32PFSG48C Configuration Flash
  - RAM hierarchical memory:
    - Each block RAM has two independent ports
    - Programmable Data Width
  - Integrated Endpoint block for PCI Express
  - Integrated Memory Controller
    - 1 Gb of DDR2 SDRAM
    - Supports access rates of up to 800Mb/s
  - Dedicated carry logic for high-speed arithmetic
  - Abundant logic resources with increased logic capacity
    - Optional shift register or distributed RAM support
    - Efficient 6-input LUTs
    - LUT with dual flip-flops
  - Four dedicated DLLs for advanced clock control
    - Phase shift input clock by 0, 90, 180, 270
    - Multiply input clock by 2 to 32
    - Divide input clock by 1 to 32
- Fully supported by Xilinx development system
  - ISE WebPACK (free download from http://www.xilinx.com)
  - ISE Design Suite
- Digital I/O Connectors
  - 48 5 volt tolerant I/O with ESD protection
  - 40 3.3 volt tolerant high speed I/O with ESD protection
- Embedded Digilent® USB JTAG Programmer
  - Allows programming from the host computer
  - Compatible with Xilinx tools, including iMpact and ChipScope
- PCI Express Bus:
  - PCIe/104 Universal Board
    - Interfaces with Type 1 or Type 2 bus
    - No re-population
  - Provides 2.5 Gbps in each direction
  - In-band interrupts and messages
  - Message Signaled Interrupt (MSI) support

1.3 Ordering Information

The FPGA35S6 series of FPGA boards is available in the following options:

Table 1: Ordering Options

Part Number	Description
FPGA35S6045HR	PCIe/104 Spartan-6 XC6SLX45T User Programmable FPGA Module
FPGA35S6100HR	PCIe/104 Spartan-6 XC6SLX100T User Programmable FPGA Module
IDAN-FPGA35S6045HR-62D	PCIe/104 Spartan-6 XC6SLX45T User Programmable FPGA Module in IDAN enclosure (62-pin connectors)
IDAN-FPGA35S6100HR-62D	PCIe/104 Spartan-6 XC6SLX100T User Programmable FPGA Module in IDAN enclosure (62-pin connectors)
IDAN-FPGA35S6045HR-68D	PCIe/104 Spartan-6 XC6SLX45T User Programmable FPGA Module in IDAN enclosure (68-pin connectors)
IDAN-FPGA35S6100HR-68D	PCIe/104 Spartan-6 XC6SLX100T User Programmable FPGA Module in IDAN enclosure (68-pin connectors)

A Starter Kit is available for any of the options, which includes the appropriate programming cable. Contact RTD Sales for more information.

The FPGA35S6 is a general use FPGA module, allowing you to design your own FPGA. It has support for custom oscillator and larger Xilinx Spartan 6 FPGAs. Please contact RTD Embedded Technologies for more information on custom FPGA35S6 products and custom FPGA designs.

The Intelligent Data Acquisition Node (IDAN®) building block can be used in just about any combination with other IDAN building blocks to create a simple but rugged 104™ stack. This module can also be incorporated in a custom-built RTD HiDAN® or HiDANplus™ High Reliability Intelligent Data Acquisition Node. Contact RTD sales for more information on our high reliability systems.

1.4 Contact Information

1.4.1 Sales Support

For sales inquiries, you can contact RTD Embedded Technologies sales via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: sales@rtd.com

1.4.2 Technical Support

If you are having problems with your system, please try the steps in the Troubleshooting section of this manual.

For help with this product, or any other product made by RTD, you can contact RTD Embedded Technologies technical support via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: techsupport@rtd.com

2 Specifications

2.1 Operating Conditions

Table 2: Operating Conditions

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{cc5}	5V Supply Voltage		4.75	5.25	V
V_{cc3}	3.3V Supply Voltage		n/a	n/a	V
V_{cc12}	12V Supply Voltage		n/a	n/a	V
T_a	Operating Temperature		-40	+85	C
T_s	Storage Temperature		-40	+85	C
RH	Relative Humidity	Non-Condensing	0	90%	%
MTBF	Mean Time Before Failure	Telcordia Issue 2 30°C, Ground benign, controlled FPGA35S6045HR		2,471,464	Hours

2.2 Electrical Characteristics

Table 3: Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
P	Power Consumption(1)	V_{cc5} = 5.0V		2.5		W
I_{cc}	5V Input Supply Current(1)	Active		500		mA
	PCIe/104 Bus					
	Differential Output Voltage		0.8		1.2	V
	DC Differential TX Impedance		80		120	Ω
	Differential Input Voltage		0.175		1.2	V
	DC Differential RX Impedance		80		120	Ω
	Electrical Idle Detect Threshold		65		175	mV
	Digital I/O					
V_{IH}	Input High Voltage	CN4,CN9	2.0		5.5	V
V_{IH}	Input High Voltage	CN8	2.0		3.6	V
V_{IL}	Input Low Voltage	CN4,CN8,CN9	-0.5		0.8	V
V_{OH}	Output High Voltage	I_O = -12mA CN4 CN8,CN9	2.6		3.3	V
V_{OL}	Output Low Voltage	I_O = 12mA CN4 CN8,CN9	0		0.4	V
	5V Output	CN4,CN8,CN9			200	mA
	DDR2 Interface					
	Access Rate(2)		250		800	Mb/s

Note: (1): Typical power consumption based on RTD's FPGA example.
(2): Proving by design, not production tested.

For additionally electrical characteristic of the Spartan 6 I/O refer to http://www.xilinx.com

3 Board Connection

3.1 Board Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your board in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the board at the edges, and do not touch the components or connectors. Handle the board in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

3.2 Physical Characteristics

STEP model is available upon request; contact RTD Tech Support for more information.

- Weight: Approximately 63.5 g (0.14 lbs.)
- Dimensions: 90.17 mm L x 95.89 mm W (3.550 in L x 3.775 in W)

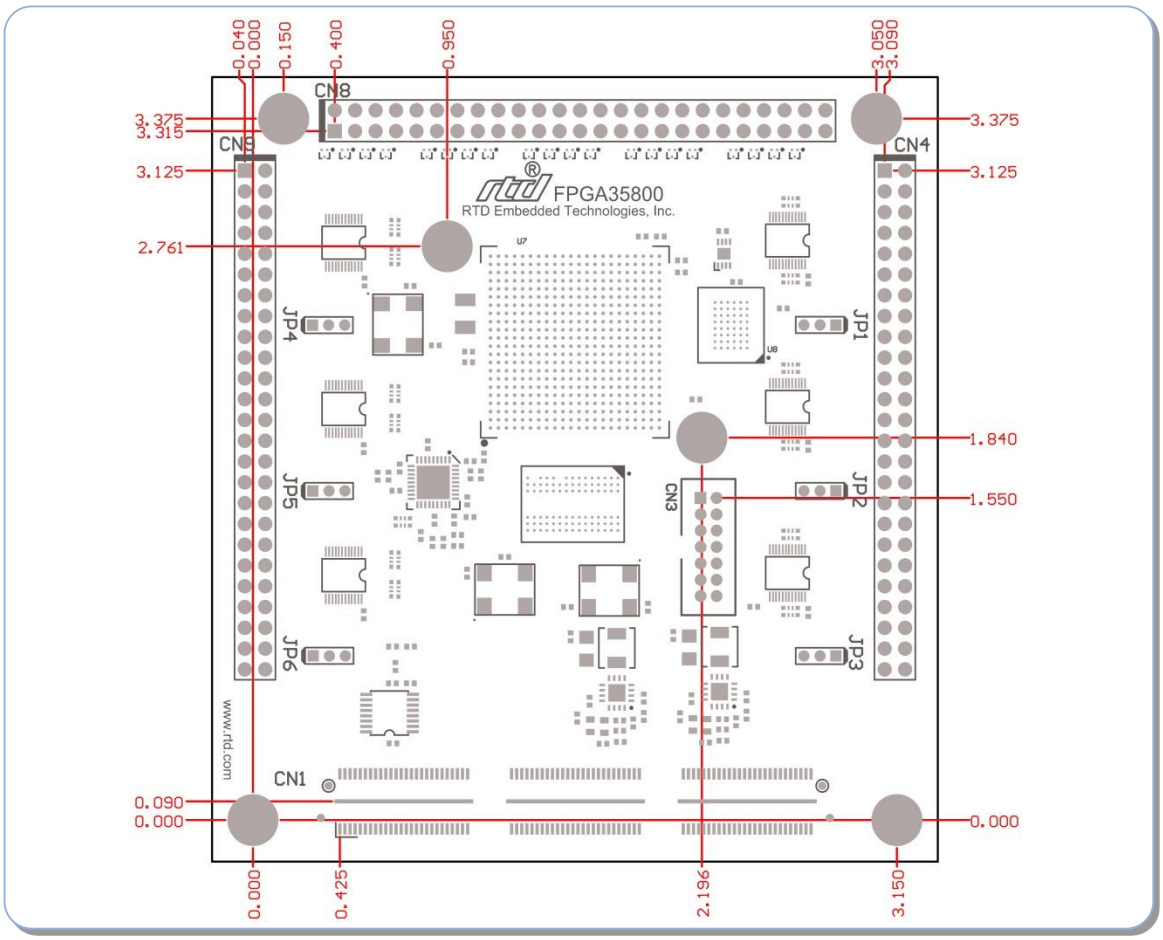

Figure 1: Board Dimensions

3.3 Connectors and Jumpers

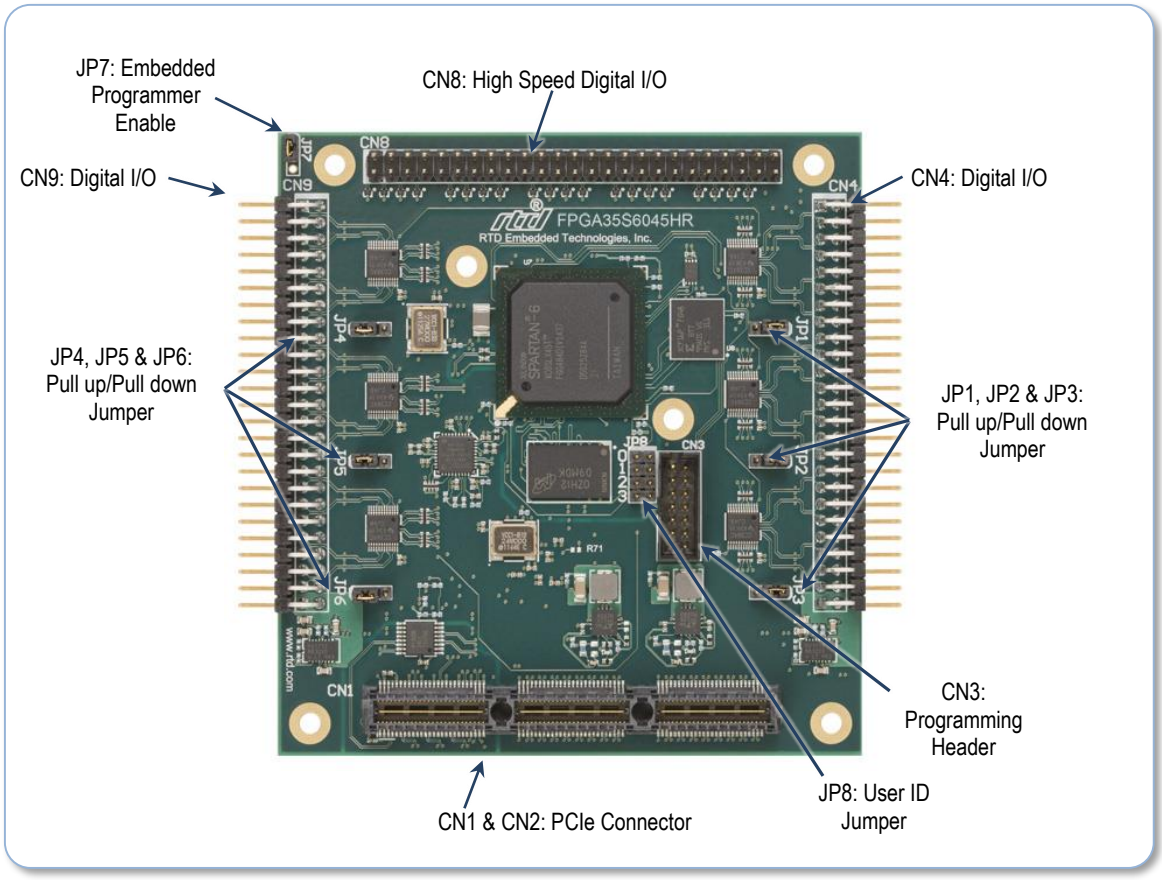

Figure 2: Board Connections

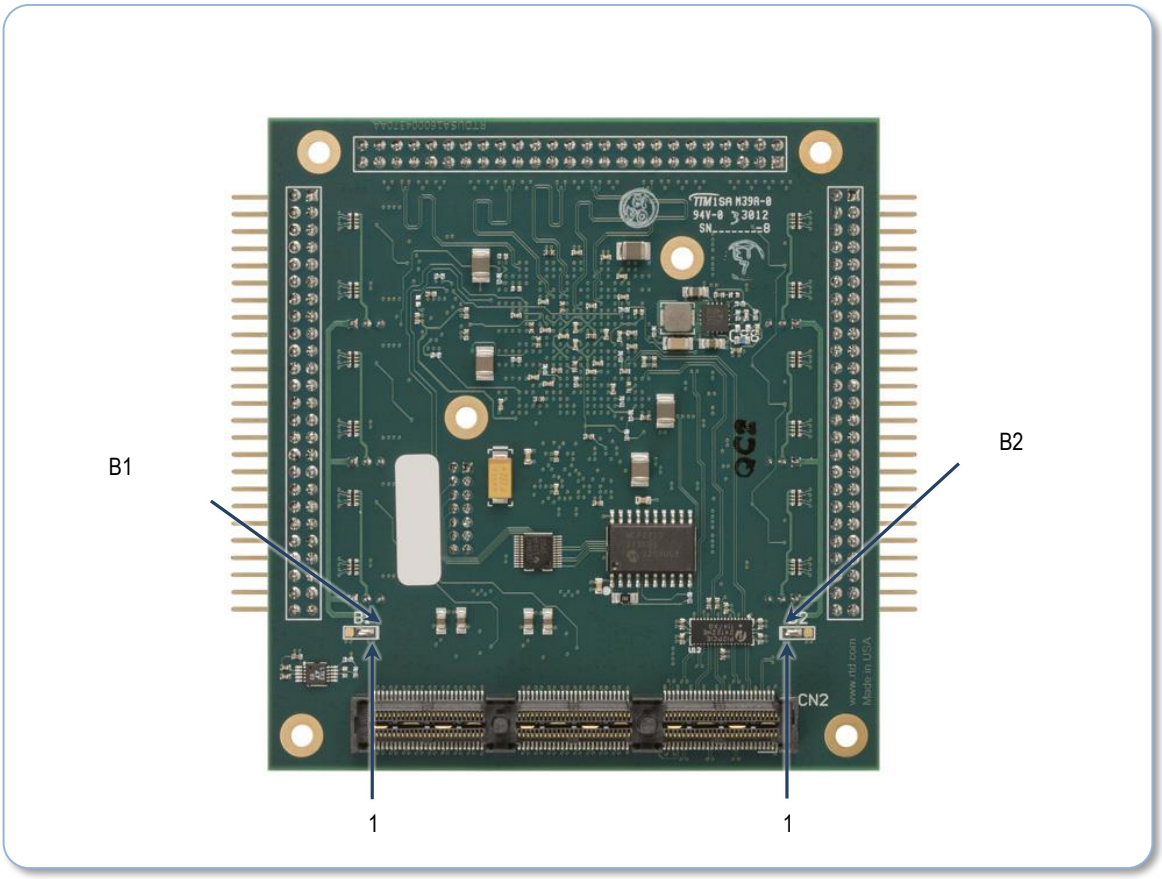

Figure 3: Bottom Solder Jumper Locations

3.3.1 External I/O Connectors

CN3: Xilinx JTAG Programming Header

Connector CN3 provides a connection to the Xilinx JTAG programming header. The pin assignment for CN3 is shown below. This connector header mates with the Xilinx OEM programming cable.

Table 4: CN3 Programming Header

3.3V VRef	2	1	GND
TMS	4	3	GND
TCK	6	5	GND
TDO	8	7	GND
TDI	10	9	GND
N/C	12	11	GND
N/C	14	13	GND

CN8: High Speed Digital I/O Connector

Connector Part #: SAMTEC TSW-125-08-S-D-RA **Mating Connector:** FCI 65043-012 LF

Connector CN8 provides 40 digital I/O lines, along with a +5V pin and ground pins. These signals are 3.3V tolerant. The signal names reflect the signal names I n the Xilinx UCF file with the device pin out.

CN8 is attached to Bank 1, and supports any of the Spartan 6 I/O Standards that use a 3.3V V_{CCO} and no reference voltage. This includes LVTTL, LVCMOS33 input and output, and LVDS_33 input. LVDS output is not supported in Bank 1.

Table 5: CN8 I/O Pin Assignments

Port2_n[0]	2	1	Port2_p[0]
Port2_n[1]	4	3	Port2_p[1]
Port2_n[2]	6	5	Port2_p[2]
Port2_n[3]	8	7	Port2_p[3]
GND	10	9	GND
Port2_n[4]	12	11	Port2_p[4]
Port2_n[5]	14	13	Port2_p[5]
Port2_n[6]	16	15	Port2_p[6]
Port2_n[7]	18	17	Port2_p[7]
GND	20	19	GND
Port2_n[8]	22	21	Port2_p[8]
Port2_n[9]	24	23	Port2_p[9]
Port2_n[10]	26	25	Port2_p[10]
Port2_n[11]	28	27	Port2_p[11]
GND	30	29	GND
Port2_n[12]	32	31	Port2_p[12]
Port2_n[13]	34	33	Port2_p[13]
Port2_n[14]	36	35	Port2_p[14]
Port2_n[15]	38	37	Port2_p[15]
GND	40	39	GND
Port2_n[16]	42	41	Port2_p[16]
Port2_n[17]	44	43	Port2_p[17]
Port2_n[18]	46	45	Port2_p[18]
Port2_n[19]	48	47	Port2_p[19]
GND	50	49	+5V

CN4 & CN9: Digital I/O Connector

Connector Part #: SAMTEC TSW-125-08-S-D-RA **Mating Connector:** FCI 65043-012 LF

Connectors CN4 and CN9 each provide 24 digital I/O lines, along with a +5V pin and ground pins. All I/O have pull up/pull down resistors that are controlled by jumper options, also shown in the table. These signals are 5V tolerant. The signal names reflect the signal names I n the Xilinx UCF file with the device pin out.

CN4 and CN9 are attached to Bank 2 and 0 respectively, and support any of the Spartan 6 I/O Standards that use a 3.3V V_{CCO} and no reference voltage. This includes LVTTL, LVCMOS33, and LVDS_33 input and output.

Table 6: CN4 I/O Pin Assignments

GND	2	1	port0_p[0]	JP1
GND	4	3	port0_n[0]	
GND	6	5	port0_p[1]	
GND	8	7	port0_n[1]	
GND	10	9	port0_p[2]	
GND	12	11	port0_n[2]	
GND	14	13	port0_p[3]	
GND	16	15	port0_n[3]	
GND	18	17	port0_p[4]	JP2
GND	20	19	port0_n[4]	
GND	22	21	port0_p[5]	
GND	24	23	port0_n[5]	
GND	26	25	port0_p[6]	
GND	28	27	port0_n[6]	
GND	30	29	port0_p[7]	
GND	32	31	port0_n[7]	
GND	34	33	port0_p[8]	JP3
GND	36	35	port0_n[8]	
GND	38	37	port0_p[9]	
GND	40	39	port0_n[9]	
GND	42	41	port0_p[10]	
GND	44	43	port0_n[10]	
GND	46	45	port0_p[11]	
GND	48	47	port0_n[11]	
GND	50	49	+5V	

Table 7: CN9 I/O Pin Assignments

GND	2	1	port1_p[0]	JP4
GND	4	3	port1_n[0]	
GND	6	5	port1_p[1]	
GND	8	7	port1_n[1]	
GND	10	9	port1_p[2]	
GND	12	11	port1_n[2]	
GND	14	13	port1_p[3]	
GND	16	15	port1_n[3]	
GND	18	17	port1_p[4]	JP5
GND	20	19	port1_n[4]	
GND	22	21	port1_p[5]	
GND	24	23	port1_n[5]	
GND	26	25	port1_p[6]	
GND	28	27	port1_n[6]	
GND	30	29	port1_p[7]	
GND	32	31	port1_n[7]	
GND	34	33	port1_p[8]	JP6
GND	36	35	port1_n[8]	
GND	38	37	port1_p[9]	
GND	40	39	port1_n[9]	
GND	42	41	port1_p[10]	
GND	44	43	port1_n[10]	
GND	46	45	port1_p[11]	
GND	48	47	port1_n[11]	
GND	50	49	+5V	

3.3.2 BUS CONNECTORS

CN1 (Top) & CN2 (Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 33)

The FPGA35S6 is a "Universal" board, and can connect to either a Type 1 or Type 2 PCIe/104 connector.

3.3.3 JUMPERS

JP1, JP2, JP3, JP4, JP5, & JP6: Pull up/Pull down Jumper

JP1, JP2, JP3, JP4, JP5, and JP6 are 3-pin two position jumpers that are used to set pull up or pull downs options on the I/O signal lines of CN4 and C5. Refer to Table 6 and Table 7 to determine which I/O pins are effected by each jumper.

Table 8: Pull up/Pull down Jumper options

Setting	Description
1-2	I/O is pulled up to 3.3V or 5V (Set by B1 and B2)
2-3	I/O is pulled down to GND
No Jumper	I/O has no pull up/pull down

JP7: Embedded Programmer Enable

This jumper is used to enable the embedded programmer to the JTAG chain. See Section 5.7 on page 28 for more details. The board can be programmed from and external programmer with this jumper in either position.

Table 9: JP7 – Embedded Programmer Enable

Setting	Description
1-2	Enabled embedded programmer
2-3 or open	Disables embedded programmer

JP8: User ID Jumper

The User ID Jumper is a four position, user defined jumper block. The jumpers can be read by the FPGA. An installed jumper results in a logic low, and an open jumper results in a logic high.

Table 10: JP8 – User ID Jumper

Position	Description
1-2	User ID bit 0
3-4	User ID bit 1
5-6	User ID bit 2
7-8	User ID bit 3

3.3.1 SOLDER JUMPERS

B1: Pull up Voltage

Solder jumper B1 are used to set the pull up voltage for JP1, JP2 and JP3.

Table 11: B1 Pull up Voltage

Setting	Description
1-2	Sets Pull up voltage to 3.3V
2-3	Sets Pull up voltage to 5V

B2: Pull up Voltage

Solder jumper B1 are used to set the pull up voltage for JP4, JP5 and JP6.

Table 12: B2 Pull up Voltage

Setting	Description
1-2	Sets Pull up voltage to 3.3V
2-3	Sets Pull up voltage to 5V

3.4 Steps for Installing

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the PC/104 system or stack.
3. Select and install stand-offs to properly position the module on the stack.
4. Remove the module from its anti-static bag.
5. Check that pins of the bus connector are properly positioned.
6. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
7. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
8. Gently and evenly press the module onto the PC/104 stack.
9. If any boards are to be stacked above this module, install them.
10. Attach any necessary cables to the PC/104 stack.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

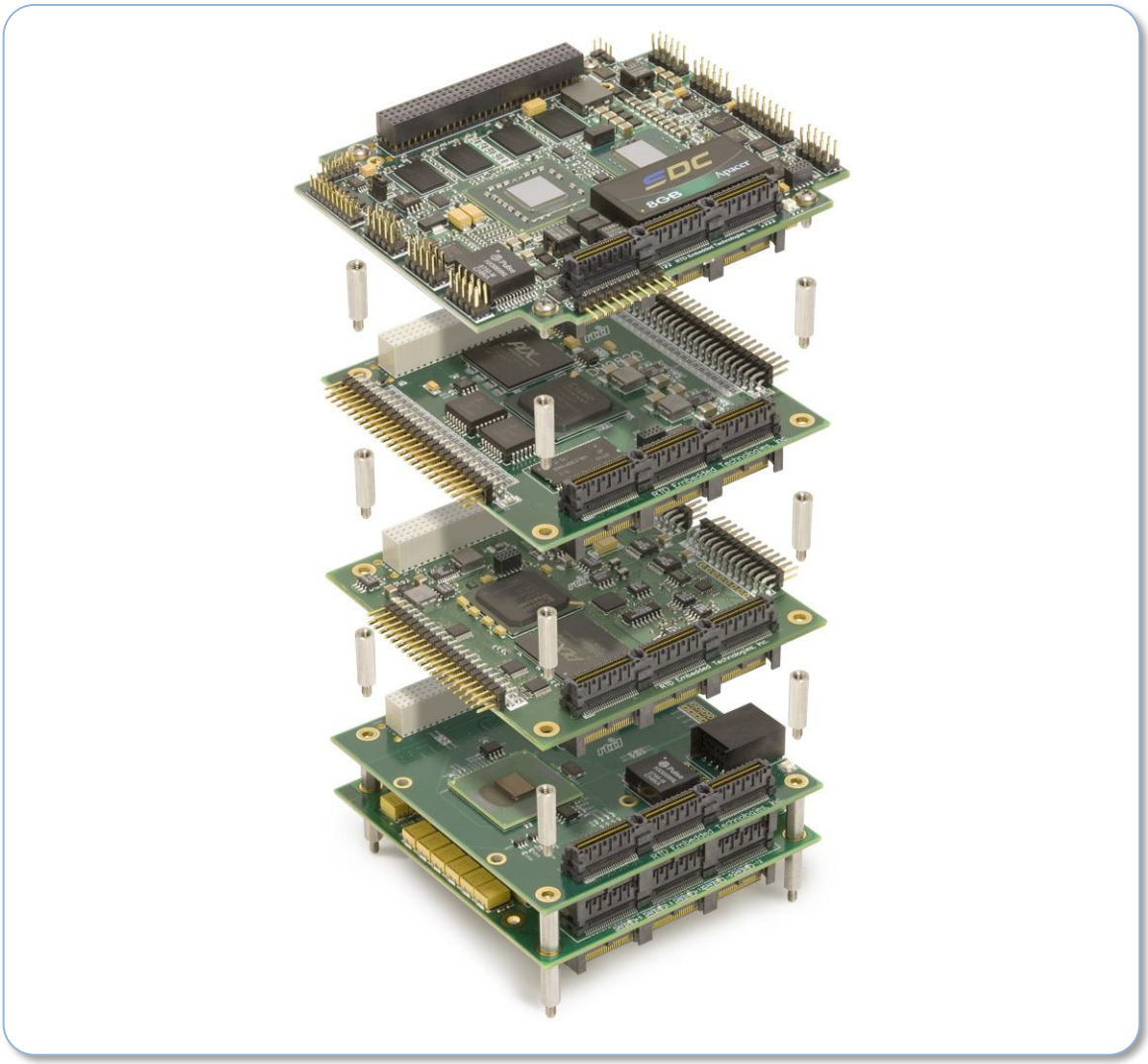

Figure 4: Example 104™ Stack

4 IDAN Connections

4.1 Module Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your module in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the module by the aluminum enclosure, and do not touch the components or connectors. Handle the module in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

4.2 Physical Characteristics

- Weight: Approximately 0.42 Kg (0.92 lbs.)
- Dimensions: 152mm L x 130mm W x 34mm H (5.983" L x 5.117" W x 1.339" H)

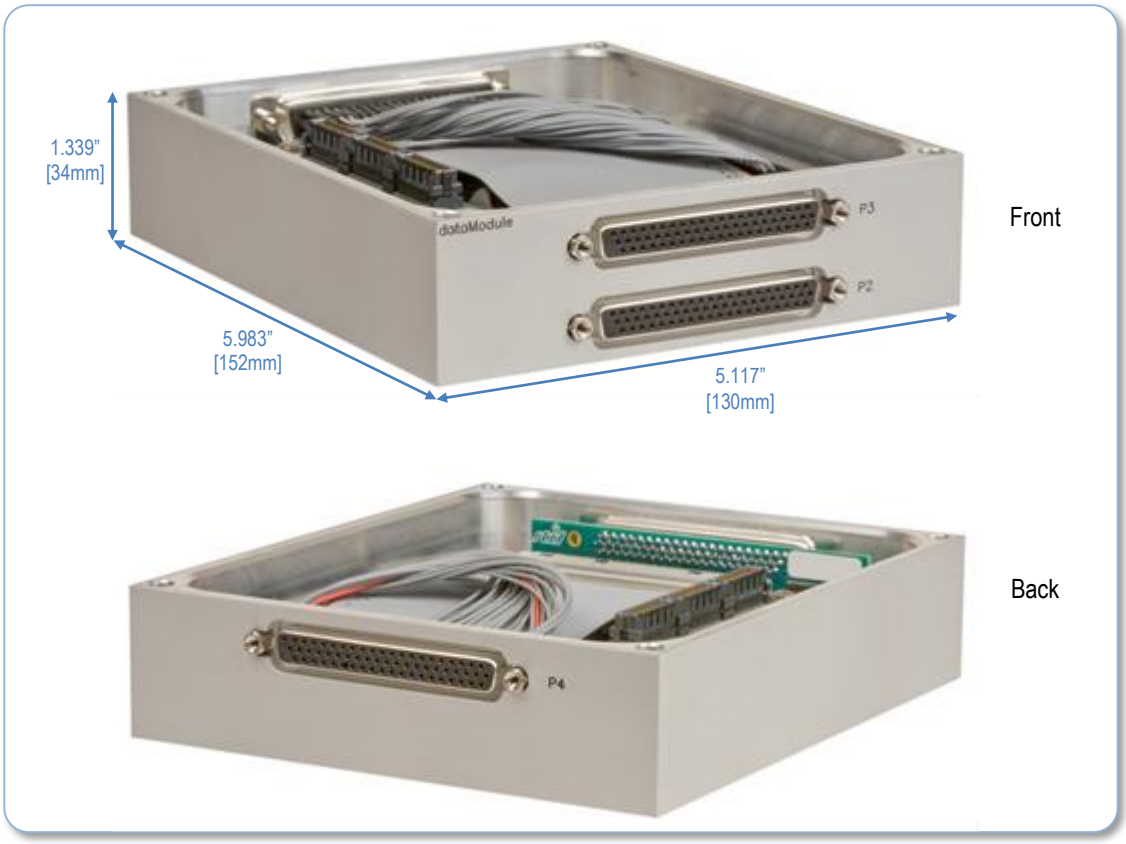

Figure 5: IDAN Dimensions (IDAN-FPGA35S6xxxHR-62D shown)

4.3 Connectors and Jumpers

P2 & P3: Digital I/O Connector

Table 13: Connector Part Numbers

RTD Order Part Number	Connector Receptacle (Manufacturer: Part Number)	Mating Connector Plug (Manufacturer: Part Number)
IDAN-FPGA35S6xxxHR-62D	VALCONN: HDB-62S	VALCONN: HDB-62P
IDAN-FPGA35S6xxxHR-68D	AMP / TE Connectivity: 749070-7	AMP: 786090-7 *(IDC crimp), or* TE Connectivity: 5786090-7

Connectors P2 and P3 each provide 24 digital I/O lines, along with a +5V pin and ground pins. All I/O have pull up/pull down resistors that are controlled by jumper options, also shown in the table. These signals are 5V tolerant. The signal names reflect the signal names I n the Xilinx UCF file with the device pin out.

P2 and P3 are attached to Bank 2 and 0 respectively, and support any of the Spartan 6 I/O Standards that use a 3.3V V_{CCO} and no reference voltage. This includes LVTTL, LVCMOS33, and LVDS_33 input and output.

Connector P2 also provides a connection to the Xilinx JTAG programming header. This connector header mates with the Xilinx OEM programming cable through an adapter cable. The adapter cable is provided when purchasing the Starter Kit.

Table 14: P2 and P3 Pin Assignments (62-pin "D")

IDAN P2 Pin				Pull	CN4
Row 1	Row 2	Row 3	Signal	Jmpr	Pin
1			port0_p[0]	JP1	1
	22		GND		2
		43	port0_n[0]		3
2			GND		4
	23		port0_p[1]		5
		44	GND		6
3			port0_n[1]		7
	24		GND		8
		45	port0_p[2]		9
4			GND		10
	25		port0_n[2]		11
		46	GND		12
5			port0_p[3]		13
	26		GND		14
		47	port0_n[3]		15
6			GND		16
	27		port0_p[4]	JP2	17
		48	GND		18
7			port0_n[4]		19
	28		GND		20
		49	port0_p[5]		21
8			GND		22
	29		port0_n[5]		23
		50	GND		24
9			port0_p[6]		25
	30		GND		26
		51	port0_n[6]		27
10			GND		28
	31		port0_p[7]		29
		52	GND		30
11			port0_n[7]		31
	32		GND		32
		53	port0_p[8]	JP3	33
12			GND		34
	33		port0_n[8]		35
		54	GND		36

IDAN P3 Pin				Pull	
Row 1	Row 2	Row 3	Signal	Jmpr	C9 Pin
1			port1_p[0]	JP4	1
	22		GND		2
		43	port1_n[0]		3
2			GND		4
	23		port1_p[1]		5
		44	GND		6
3			port1_n[1]		7
	24		GND		8
		45	port1_p[2]		9
4			GND		10
	25		port1_n[2]		11
		46	GND		12
5			port1_p[3]		13
	26		GND		14
		47	port1_n[3]		15
6			GND		16
	27		port1_p[4]	JP5	17
		48	GND		18
7			port1_n[4]		19
	28		GND		20
		49	port1_p[5]		21
8			GND		22
	29		port1_n[5]		23
		50	GND		24
9			port1_p[6]		25
	30		GND		26
		51	port1_n[6]		27
10			GND		28
	31		port1_p[7]		29
		52	GND		30
11			port1_n[7]		31
	32		GND		32
		53	port1_p[8]	JP6	33
12			GND		34
	33		port1_n[8]		35
		54	GND		36

Table 14: P2 and P3 Pin Assignments (62-pin "D")

IDAN P2 Pin				Pull	CN4
Row 1	Row 2	Row 3	Signal	Jmpr	Pin
13			port0_p[9]		37
	34		GND		38
		55	port0_n[9]		39
14			GND		40
	35		port0_p[10]		41
		56	GND		42
15			port0_n[10]		43
	36		GND		44
		57	port0_p[11]		45
16			GND		46
	37		port0_n[11]		47
		58	GND		48
17			+5V		49
	38		GND		50
		59	*Reserved*		
18			*Reserved*		
	39		*Reserved*		
		60	*Reserved*		
19			*Reserved*		
	40		*Reserved*		
		61	*Reserved*		
20			*Reserved*		
	41		*Reserved*		
		62	*Reserved*		
21			*Reserved*		
	42		*Reserved*		

IDAN P3 Pin				Pull	
Row 1	Row 2	Row 3	Signal	Jmpr	C9 Pin
13			port1_p[9]		37
	34		GND		38
		55	port1_n[9]		39
14			GND		40
	35		port1_p[10]		41
		56	GND		42
15			port1_n[10]		43
	36		GND		44
		57	port1_p[11]		45
16			GND		46
	37		port1_n[11]		47
		58	GND		48
17			+5V		49
	38		GND		50
		59	*Reserved*		
18			jtag_vref		CN3.2
	39		GND		CN3.3
		60	jtag_tms		CN3.4
19			GND		CN3.5
	40		jtag_tck		CN3.6
		61	GND		CN3.7
20			jtag_tdo		CN3.8
	41		GND		CN3.9
		62	jtag_tdi		CN3.10
21			*Reserved*		
	42		*Reserved*		

Table 15: P2 and P3 Pin Assignments (68-pin "D")

IDAN P2 Pin			Pull	CN4
Row 1	Row 2	Signal	Jmpr	Pin
1		port0_p[0]		1
	2	GND		2
3		port0_n[0]		3
	4	GND		4
5		port0_p[1]		5
	6	GND		6
7		port0_n[1]		7
	8	GND	JP1	8
9		port0_p[2]		9
	10	GND		10
11		port0_n[2]		11
	12	GND		12
13		port0_p[3]		13
	14	GND		14
15		port0_n[3]		15
	16	GND		16
17		port0_p[4]		17
	18	GND		18
19		port0_n[4]		19
	20	GND		20
21		port0_p[5]	JP2	21
	22	GND		22
23		port0_n[5]		23
	24	GND		24
25		port0_p[6]		25

IDAN P3 Pin			Pull	
Row 1	Row 2	Signal	Jmpr	C9 Pin
1		port1_p[0]		1
	2	GND		2
3		port1_n[0]		3
	4	GND		4
5		port1_p[1]		5
	6	GND		6
7		port1_n[1]		7
	8	GND	JP4	8
9		port1_p[2]		9
	10	GND		10
11		port1_n[2]		11
	12	GND		12
13		port1_p[3]		13
	14	GND		14
15		port1_n[3]		15
	16	GND		16
17		port1_p[4]		17
	18	GND		18
19		port1_n[4]		19
	20	GND		20
21		port1_p[5]	JP5	21
	22	GND		22
23		port1_n[5]		23
	24	GND		24
25		port1_p[6]		25

Table 15: P2 and P3 Pin Assignments (68-pin "D")

IDAN P2 Pin			Pull	CN4
Row 1	Row 2	Signal	Jmpr	Pin
	26	GND		26
27		port0_n[6]		27
	28	GND		28
29		port0_p[7]		29
	30	GND		30
31		port0_n[7]		31
	32	GND		32
33		port0_p[8]		33
	34	GND		34
35		port0_n[8]		35
	36	GND		36
37		port0_p[9]		37
	38	GND		38
39		port0_n[9]		39
	40	GND	JP3	40
41		port0_p[10]		41
	42	GND		42
43		port0_n[10]		43
	44	GND		44
45		port0_p[11]		45
	46	GND		46
47		port0_n[11]		47
	48	GND		48
49		+5V		49
	50	GND		50
51		*Reserved*		
	52	*Reserved*		
53		*Reserved*		
	54	*Reserved*		
55		*Reserved*		
	56	*Reserved*		
57		*Reserved*		
	58	*Reserved*		
59		*Reserved*		
	60	*Reserved*		
61		*Reserved*		
	62	*Reserved*		
63		*Reserved*		
	64	*Reserved*		
65		*Reserved*		
	66	*Reserved*		
67		*Reserved*		
	68	*Reserved*		

IDAN P3 Pin			Pull	
Row 1	Row 2	Signal	Jmpr	C9 Pin
	26	GND		26
27		port1_n[6]		27
	28	GND		28
29		port1_p[7]		29
	30	GND		30
31		port1_n[7]		31
	32	GND		32
33		port1_p[8]		33
	34	GND		34
35		port1_n[8]		35
	36	GND		36
37		port1_p[9]		37
	38	GND		38
39		port1_n[9]		39
	40	GND	JP6	40
41		port1_p[10]		41
	42	GND		42
43		port1_n[10]		43
	44	GND		44
45		port1_p[11]		45
	46	GND		46
47		port1_n[11]		47
	48	GND		48
49		+5V		49
	50	GND		50
51		*Reserved*		
	52	jtag_vref		CN3.2
53		GND		CN3.3
	54	jtag_tms		CN3.4
55		GND		CN3.5
	56	jtag_tck		CN3.6
57		GND		CN3.7
	58	jtag_tdo		CN3.8
59		GND		CN3.9
	60	jtag_tdi		CN3.10
61		*Reserved*		
	62	*Reserved*		
63		*Reserved*		
	64	*Reserved*		
65		*Reserved*		
	66	*Reserved*		
67		*Reserved*		
	68	*Reserved*		

P4: High Speed Digital I/O Connector

Connector Part #: VALCONN HDB-62S **Mating Connector:** VALCONN HDB-62P

Connector P4 provides 40 digital I/O lines, along with a +5V pin and ground pins. These signals are 3.3V tolerant. The signal names reflect the signal names I n the Xilinx UCF file with the device pin out.

P4 is attached to Bank 1, and supports any of the Spartan 6 I/O Standards that use a 3.3V V_{CCO} and no reference voltage. This includes LVTTL, LVCMOS33 input and output, and LVDS_33 input. LVDS output is not supported in Bank 1.

Table 16: P4 Pin Assignments (62-pin "D")

IDAN P4 Pin			Signal	C8 Pin
Row 1	Row 2	Row 3		
1			Port2_p[0]	1
	22		Port2_n[0]	2
		43	Port2_p[1]	3
2			Port2_n[1]	4
	23		Port2_p[2]	5
		44	Port2_n[2]	6
3			Port2_p[3]	7
	24		Port2_n[3]	8
		45	GND	9
4			GND	10
	25		Port2_p[4]	11
		46	Port2_n[4]	12
5			Port2_p[5]	13
	26		Port2_n[5]	14
		47	Port2_p[6]	15
6			Port2_n[6]	16
	27		Port2_p[7]	17
		48	Port2_n[7]	18
7			GND	19
	28		GND	20
		49	Port2_p[8]	21
8			Port2_n[8]	22
	29		Port2_p[9]	23
		50	Port2_n[9]	24
9			Port2_p[10]	25
	30		Port2_n[10]	26
		51	Port2_p[11]	27
10			Port2_n[11]	28
	31		GND	29
		52	GND	30
11			Port2_p[12]	31
	32		Port2_n[12]	32
		53	Port2_p[13]	33
12			Port2_n[13]	34
	33		Port2_p[14]	35
		54	Port2_n[14]	36
13			Port2_p[15]	37
	34		Port2_n[15]	38
		55	GND	39
14			GND	40
	35		Port2_p[16]	41
		56	Port2_n[16]	42
15			Port2_p[17]	43
	36		Port2_n[17]	44
		57	Port2_p[18]	45
16			Port2_n[18]	46
	37		Port2_p[19]	47
		58	Port2_n[19]	48
17			+5V	49
	38		GND	50
		59	*Reserved*	
18			*Reserved*	
	39		*Reserved*	
		60	*Reserved*	
19			*Reserved*	
	40		*Reserved*	
		61	*Reserved*	
20			*Reserved*	
	41		*Reserved*	

Table 16: P4 Pin Assignments (62-pin "D")

IDAN P4 Pin			Signal	C8 Pin
Row 1	Row 2	Row 3		
		62	*Reserved*	
21			*Reserved*	
	42		*Reserved*	

Table 17: P4 Pin Assignments (68-pin "D")

IDAN P2 Pin			Pull	CN4
Row 1	Row 2	Signal	Jmpr	Pin
1		Port2_p[0]		1
	2	Port2_n[0]		2
3		Port2_p[1]		3
	4	Port2_n[1]		4
5		Port2_p[2]		5
	6	Port2_n[2]		6
7		Port2_p[3]		7
	8	Port2_n[3]		8
9		GND		9
	10	GND		10
11		Port2_p[4]		11
	12	Port2_n[4]		12
13		Port2_p[5]		13
	14	Port2_n[5]		14
15		Port2_p[6]		15
	16	Port2_n[6]		16
17		Port2_p[7]		17
	18	Port2_n[7]		18
19		GND		19
	20	GND		20
21		Port2_p[8]		21
	22	Port2_n[8]		22
23		Port2_p[9]		23
	24	Port2_n[9]		24
25		Port2_p[10]		25
	26	Port2_n[10]		26
27		Port2_p[11]		27
	28	Port2_n[11]		28
29		GND		29
	30	GND		30
31		Port2_p[12]		31
	32	Port2_n[12]		32
33		Port2_p[13]		33
	34	Port2_n[13]		34
35		Port2_p[14]		35
	36	Port2_n[14]		36
37		Port2_p[15]		37
	38	Port2_n[15]		38
39		GND		39
	40	GND		40
41		Port2_p[16]		41
	42	Port2_n[16]		42
43		Port2_p[17]		43
	44	Port2_n[17]		44
45		Port2_p[18]		45
	46	Port2_n[18]		46
47		Port2_p[19]		47
	48	Port2_n[19]		48
49		+5V		49
	50	GND		50
51-68		RESERVED		-

4.3.1 BUS CONNECTORS

CN1 (Top) & CN2 (Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 33)

The FPGA35S6 is a "Universal" board, and can connect to either a Type 1 or Type 2 PCIe/104 connector.

4.3.2 JUMPERS

JP1, JP2, JP3, JP4, JP5, & JP6: Pull up/Pull down Jumper

JP1, JP2, JP3, JP4, JP5, and JP6 are 3-pin two position jumpers that are used to set pull up or pull downs options on the I/O signal lines of CN4 and C5. Refer to Table 14 and Table 16 to determine which I/O pins are effected by each jumper.

Table 18: Pull up/Pull down Jumper options

Setting	Description
1-2	I/O is pulled up to 3.3V or 5V (Set by B1 and B2)
2-3	I/O is pulled down to GND
No Jumper	I/O has no pull up/pull down

JP7: Embedded Programmer Enable

This jumper is used to enable the embedded programmer to the JTAG chain. See Section 5.7 on page 28 for more details. The board can be programmed from and external programmer with this jumper in either position.

Table 19: B1 Pull up Voltage

Setting	Description
1-2	Enabled embedded programmer
2-3 or open	Disables embedded programmer

JP8: User ID Jumper

The User ID Jumper is a four position, user defined jumper block. The jumpers can be read by the FPGA. An installed jumper results in a logic low, and an open jumper results in a logic high.

Table 20: JP8 – User ID Jumper

Position	Description
1-2	User ID bit 0
3-4	User ID bit 1
5-6	User ID bit 2
7-8	User ID bit 3

4.3.3 SOLDER JUMPERS

B1: Pull up Voltage

Solder jumper B1 are used to set the pull up voltage for JP1, JP2 and JP3.

Table 21: B1 Pull up Voltage

Setting	Description
1-2	Sets Pull up voltage to 3.3V
2-3	Sets Pull up voltage to 5V

B2: Pull up Voltage

Solder jumper B1 are used to set the pull up voltage for JP4, JP5 and JP6.

Table 22: B2 Pull up Voltage

Setting	Description
1-2	Sets Pull up voltage to 3.3V
2-3	Sets Pull up voltage to 5V

4.4 Steps for Installing

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the IDAN system.
3. Remove the module from its anti-static bag.
4. Check that pins of the bus connector are properly positioned.
5. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
6. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
7. Gently and evenly press the module onto the IDAN system.
8. If any boards are to be stacked above this module, install them.
9. Finish assembling the IDAN stack by installing screws of an appropriate length.
10. Attach any necessary cables to the IDAN system.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

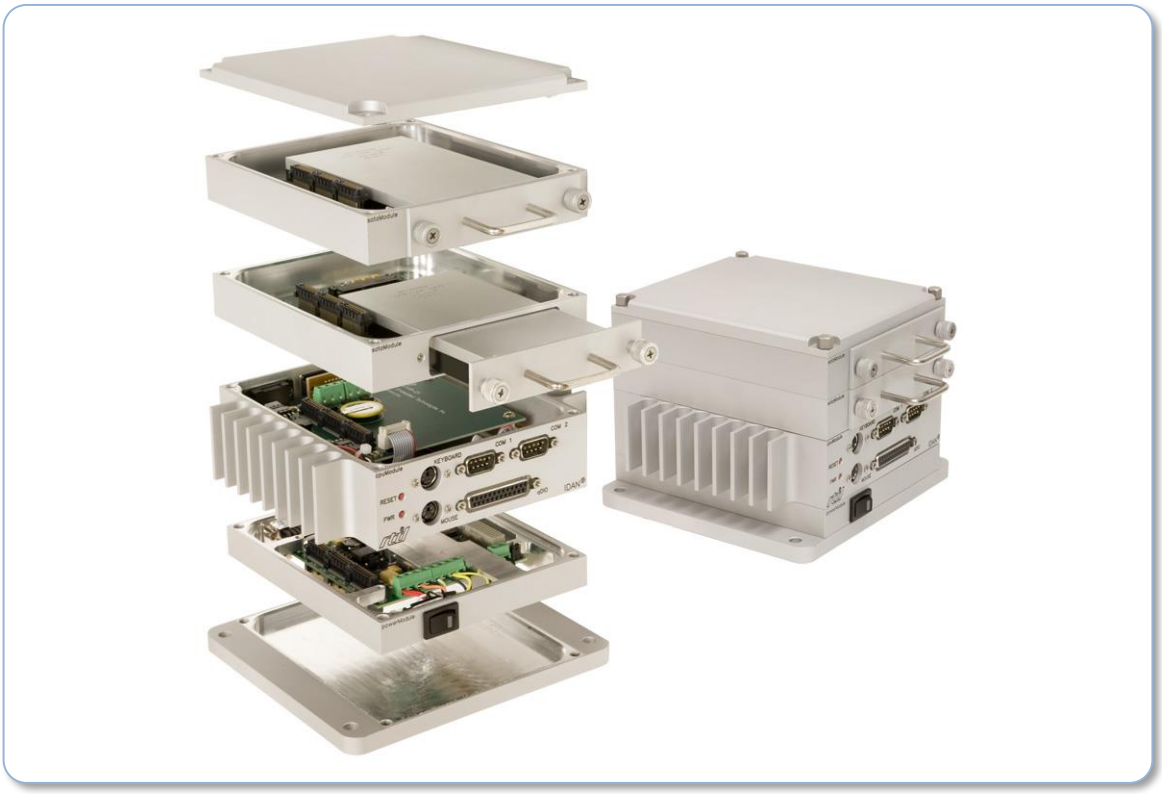

Figure 6: Example IDAN System

5 Functional Description

5.1 Block Diagram

The Figure below shows the functional block diagram of the FPGA35S6. The various parts of the block diagram are discussed in the following sections.

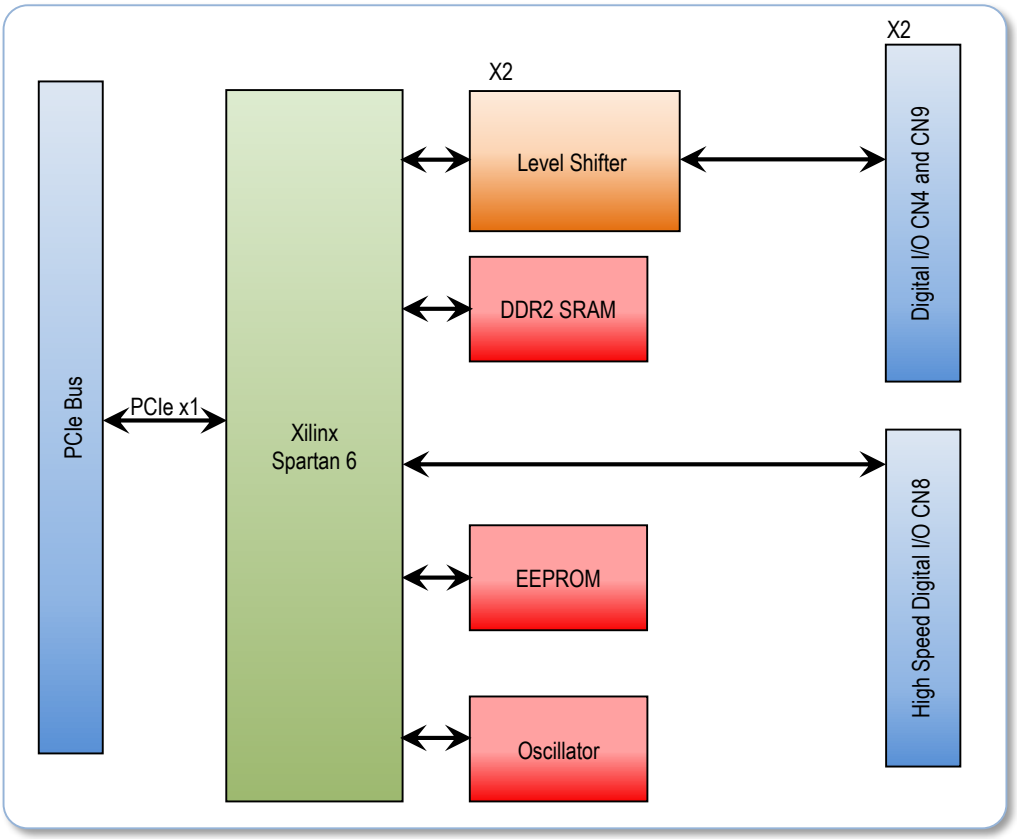

Figure 7: FPGA35S6 Block Diagram

5.2 Configuration Flash

The FPGA35S6 includes a Configuration Flash that is sized for the FPGA. At power up, the FPGA design is loaded from the Configuration Flash. The Configuration Flash can be programmed through either the Embedded Digilent® USB JTAG Programmer, or CN3: Xilinx JTAG Programming Header.

5.3 Oscillator

The FPGA35S6 features a 27 MHz oscillator for clock based operations in the FPGA.

5.4 EEPROM

The FPGA35S6 features a 256 x 16 SPI EEPROM, ATMEL AT93C66A. For information on the AT93C66A refer to http://www.atmel.com/

5.5 DDR2 SRAM

The FPGA35S6 features a 1Gb DDR2 SRAM, MT47H64M16HR 25E. This is interface to the Spartan 6 FPGA using Xilinx Memory Interface Generators (MIG) core. The example FPGA code has demonstrated how to use this core in a FPGA design.

5.6 Digital I/O

The FPGA35S6 digital I/O on connectors CN4 and CN9 use the circuitry shown below to level shift the input voltage from 5V to 3.3V allowing the I/O on these connectors to be 5V tolerant.

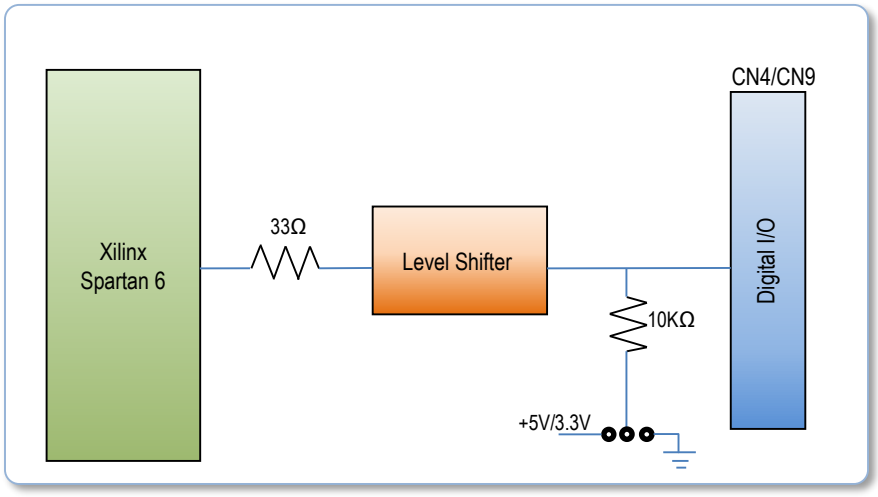

Figure 8: CN4/CN9 Digital I/O Circuitry

5.7 Embedded Digilent® USB JTAG Programmer

This FPGA board includes an embedded Digilent ® JTAG programming module. It connects to the host through the USB connections on the PCIe Bus connectors. A USB hub is also provided for lane repopulation. The programming module is compatible with all Xilinx tools, including iMpact and ChipScope (www.xilinx.com). It is also supported by Digilent's Adept software package (www.digilentinc.com).

In order to use the embedded programmer, JP7 must be installed in the 1-2 position. This attaches the programmer to the JTAG chain. CN3 can always be used regardless of whether or not JP1 is installed.

The embedded programmer has a user string of "RTD" followed by the serial number of the board. This can be used to differentiate the programmers if there are multiple boards in the system.

6 Register Address Space

This is the register address space for the example FPGA that is given with the FPGA35S6.

6.1 Identifying the Board

The FPGA35S6 Example shows up in standard PCI Configuration space as a PCI device. It can be positively identified as shown in the Table below.

Table 23: Identifying the FPGA35S6

Configuration Space Offset	Register Description	Value
0x00	Vendor ID	0x1435
0x02	Device ID	0x5800

6.2 BAR0 – FPGA Example Register Map

Table 24: FPGA Example Register Map

Offset	0x03	0x02	0x01	0x00
0x00	R_ID			
0x04	R_STATUS			
0x08	R_EEPROM			
0x0C	R_USER_ID			
0x10	R_PORT0_IN			
0x14	R_PORT0_OUT			
0x18	R_PORT0_DIR			
0x20	R_PORT1_IN			
0x24	R_PORT1_OUT			
0x28	R_PORT1_DIR			
0x30	R_PORT2L_IN			
0x34	R_PORT2L_OUT			
0x38	R_PORT2L_DIR			
0x40	R_PORT2H_IN			
0x44	R_PORT2H_OUT			
0x48	R_PORT2H_DIR			
0x50	R_DDR_RD_DATA			
0x54	R_DDR_WR_DATA			
0x58	R_DDR_ADDR			
0x5C	R_DDR_STATUS			
0x60	R_CLK_27_1			
0x64	R_CLK_27_2			

6.2.1 R_ID (READ)

This is a register that identifies the board.

0x12345678 is the identification of the example code

6.2.2 R_STATUS (READ)

This is a status register for power good (pgood) for the power supplies and serial out from the EEPROM

B0: EEPROM Serial out

B4: 1.2V pgood

B5: 1.8V pgood

B6: 3.3V pgood

6.2.3 R_EEPROM (READ/WRITE)

This register has the outputs to the EEPROM.

B0: EEPROM Serial Clock

B1: EEPROM Serial Input

B2: EEPROM Chip Select

6.2.4 R_USER_ID (READ)

This register shows the status of the User ID Jumpers

B0: User ID 0 Jumper. 0 = Open, 1 = Closed

B1: User ID 1 Jumper. 0 = Open, 1 = Closed

B2: User ID 2 Jumper. 0 = Open, 1 = Closed

B3: User ID 3 Jumper. 0 = Open, 1 = Closed

6.2.5 R_PORT0_IN (READ)

This is the input register for the port0. This reads the current value the I/O.

6.2.6 R_PORT0_OUT (WRITE)

This is the output register for the port0. The value to be output, direction must be set to output.

6.2.7 R_PORT0_DIR (WRITE)

This is the direction register for port0. Indicates the direction of each pin '0' = input '1' = output

6.2.8 R_PORT1_IN (READ)

This is the input register for the port1. This reads the current value the I/O.

6.2.9 R_PORT1_OUT (WRITE)

This is the output register for the port1. The value to be output, direction must be set to output.

6.2.10 R_PORT1_DIR (READ/WRITE)

This is the direction register for port1. Indicates the direction of each pin '0' = input '1' = output

6.2.11 R_PORT2L_IN (READ)

This is the input register for the port2 low, port2_[0]…port2_[15]. This reads the current value the I/O.

6.2.12 R_PORT2L_OUT (WRITE)

This is the output register for the port2 low, port2_[0]…port2_[15]. The value to be output, direction must be set to output.

6.2.13 R_PORT2L_DIR (READ/WRITE)

This is the direction register for port2 low, port2_[0]…port2_[15]. Indicates the direction of each pin '0' = input '1' = output

6.2.14 R_PORT2H_IN (READ)

This is the input register for the port2 high, port2_[16]…port2_[19]. This reads the current value the I/O.

6.2.15 R_PORT2H_OUT (WRITE)

This is the output register for the port2 high, port2_[16]…port2_[19]. The value to be output, direction must be set to output.

6.2.16 R_PORT2H_DIR (READ/WRITE)

This is the direction register for port2 high, port2_[16]…port2_[19]. Indicates the direction of each pin '0' = input '1' = output

6.2.17 R_DDR_RD_DATA (READ)

Reads the data of the DDR2 SRAM at R_DDR_ADDR location

A read is performed by writing address to R_DDR_ADDR.

6.2.18 R_DDR_WR_DATA (READ/WRITE)

Writes data in registry to location R_DDR_ADDR of the DDR2 SRAM

6.2.19 R_DDR_ADDR (READ/WRITE)

Address pointer of the DDR2 SRAM.

6.2.20 R_DDR_STATUS (READ)

This is a status register for the DDR2 memory interface.

B0: Read error

B1: Read overflow

B2: Read empty

B3: Read full

B4: Write error

B5: Write underrun

B6: Write empty

B7: Write full

B[14:8]: Read count

B[22:16]: Write count

B[24]: Command full

B[25]: Command empty

B[31]: Calibration done

7 Troubleshooting

If you are having problems with your system, please try the following initial steps:

- **Simplify the System** – Remove modules one at a time from your system to see if there is a specific module that is causing a problem. Perform you troubleshooting with the least number of modules in the system possible.

- **Swap Components** – Try replacing parts in the system one at a time with similar parts to determine if a part is faulty or if a type of part is configured incorrectly.

If problems persist, or you have questions about configuring this product, contact RTD Embedded Technologies via the following methods:

Phone: +1-814-234-8087
E-Mail: techsupport@rtd.com

Be sure to check the RTD web site (http://www.rtd.com) frequently for product updates, including newer versions of the board manual and application software.

8 Additional Information

8.1 PC/104 Specifications

A copy of the latest PC/104 specifications can be found on the webpage for the PC/104 Embedded Consortium:

www.pc104.org

8.2 PCI and PCI Express Specification

A copy of the latest PCI and PCI Express specifications can be found on the webpage for the PCI Special Interest Group:

www.pcisig.com

9 Limited Warranty

RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD Embedded Technologies, Inc. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, RTD Embedded Technologies will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to RTD Embedded Technologies. All replaced parts and products become the property of RTD Embedded Technologies. Before returning any product for repair, customers are required to contact the factory for a Return Material Authorization (RMA) number.

This limited warranty does not extend to any products which have been damaged as a result of accident, misuse, abuse (such as: use of incorrect input voltages, improper or insufficient ventilation, failure to follow the operating instructions that are provided by RTD Embedded Technologies, “acts of God” or other contingencies beyond the control of RTD Embedded Technologies), or as a result of service or modification by anyone other than RTD Embedded Technologies. Except as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranties of merchantability and fitness for a particular purpose, and RTD Embedded Technologies expressly disclaims all warranties not stated herein. All implied warranties, including implied warranties for merchantability and fitness for a particular purpose, are limited to the duration of this warranty. In the event the product is not free from defects as warranted above, the purchaser's sole remedy shall be repair or replacement as provided above. Under no circumstances will RTD Embedded Technologies be liable to the purchaser or any user for any damages, including any incidental or consequential damages, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

Some states do not allow the exclusion or limitation of incidental or consequential damages for consumer products, and some states do not allow limitations on how long an implied warranty lasts, so the above limitations or exclusions may not apply to you.

This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

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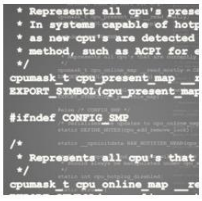

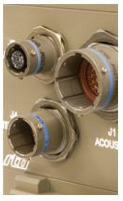
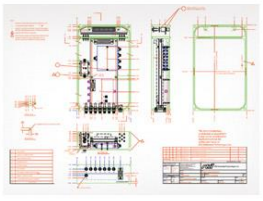

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