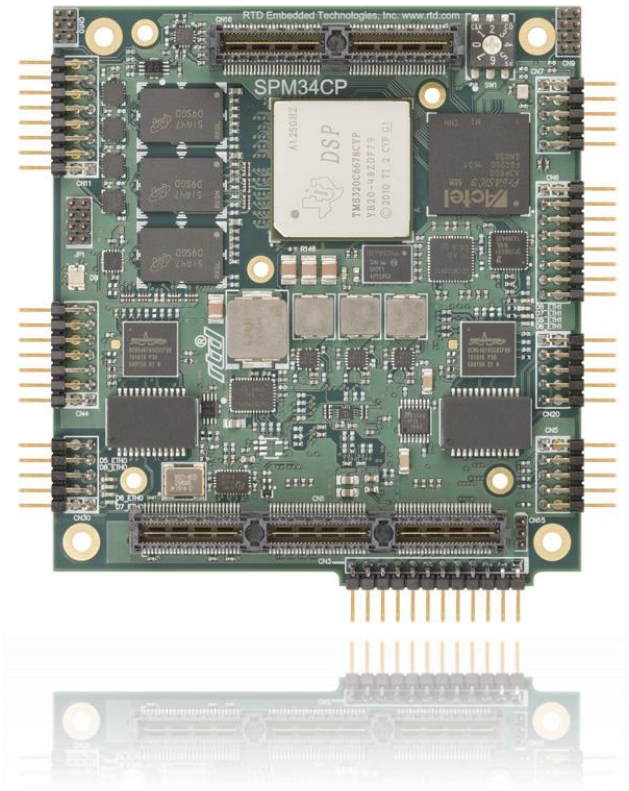
SPM34CP, SPM35CP

PCI Express Multicore Fixed and Floating-Point DSP

User's Manual

BDM-610030006 Rev. B



RTD Embedded Technologies, Inc.
AS9100 and ISO 9001 Certified

RTD Embedded Technologies, Inc.
103 Innovation Boulevard
State College, PA 16803 USA
Telephone: 814-234-8087
Fax: 814-234-5218

www.rtd.com

sales@rtd.com
techsupport@rtd.com

Revision History

Rev A	Initial Release
Rev B	Throughout: Add SPM35CP Section 2.1: Add MTBF for SPM34CP Section 3.5.3: The factory loaded program for testing boot selector switch position 4 has been modified from LED color green to white

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1 Introduction

1.1 Product Overview

Based on the Texas Instruments TMS320C66x, RTD's SPM34CP and SPM35CP dspModules are high performance fixed/floating point embedded DSP controllers designed around the PCIe/104 stackable bus structure. The onboard DSP chip supports high-performance signal processing applications such as mission critical, imaging, test, and automation. Deterministic processing allows the DSP to outperform general purpose processors for time-critical applications. The C6678 platform is power-efficient and easy to use. The C66x CorePac DSP is fully backward compatible with TI's existing C6000 family of fixed and floating point DSPs.

The DSP chip has several high-speed data connections to the outside including PCI Express and Gigabit Ethernet. Onboard flash permits true stand-alone operation of the DSP without a host or as a high-speed accelerator to an analog front-end module, while the PCI Express connector alternatively permits the DSP to act a co-processor to a PCIe/104 host cpuModules. This is achieved over a PCIe x2 link on the SPM34CP, which requires that the host cpuModules has PCIe/104 Type 2 connectors. The SPM34CP has a universal bus and utilizes PCIe x1 connections, so it may be connected to either a PCIe/104 Type 1 or Type 2 host.

Additional hardware features include one RS-232/422/485 serial port as well as fourteen 5V-tolerant 3VTTL general purpose I/O.

When paired with an RTD cpuModule and a high-speed signal source/drain (e.g. RTD's DM35418HR dataModule), the result is a complete high-speed data acquisition, signal processing, and decision-making system. The Gigabit Ethernet connections, or stackable Serial RapidIO® (which boasts four configurable lanes), are ideal for high-speed data transfers between the DSP and the mated source/drain board or system.

The SPM34CP and SPM35CP are available in dual- and octal-core configurations, and includes a suite of matching host-side and DSP-side libraries permitting single and multi-threaded applications for all on-board features.

1.2 Board Features

- PCI/104 form factor
- PCIe/104 stackable bus structure
  - PCIe Type 2 expansion bus (SPM34CP only)
  - PCIe Universal expansion bus (SPM35CP only)
- PCIe x2 interface (Gen 2, 5 GT/s)
  - Compatible with RTD's Intel Core i7-based cpuModules
- **Texas Instruments TMS320C66x™ DSP Core Subsystems (C66x CorePacs)**
  - Built for real-time, deterministic processing
  - 1.25 GHz C66x Fixed/Floating-Point CPU with up to 8 Cores
  - 32 KByte Level 1 Program (L1P) cache per core
  - 32 KByte Level 2 Data (L2D) cache per core
  - 512 KByte Local Level 2 cache per core
  - 4096 KByte On-chip RAM
  - Support for User TI Code Composer Studio
  - The C66x CorePac is fully backward compatible with TI's existing C6000 family of fixed and floating point DSPs
- 2GB or 4GB DDR3 SDRAM
  - Surface-mounted for maximum reliability
  - Features robust Error Code Correction (ECC)
- Stand-alone or CPU Co-Processor Operating Modes
  - 16MB SPI Flash for user bootloaders
  - Power connector for stand-alone operation
  - Co-processor operation supported with:
    - One PCI Express (PCIe) x2 Upstream Link to a PCIe/104 Type 2 cpuModule (SPM34CP only)
    - One PCI Express (PCIe) x1 Upstream Link to a PCIe/104 Type 1 or Type 2 cpuModule (SPM35CP only)
  - Ethernet Boot
  - Switch selectable
- Four lanes of Serial RapidIO®
  - Up to 5 GT/s operation per lane
  - Supports Direct I/O, Message Passing
  - Link configurations configurable as four x1, two x2, one x4, and two x1 + one x2
- Gigabit Ethernet Switch Subsystem
  - Supports 10/100/1000 Mbps operation
  - Single controller with two switched connections
  - Hardware flow control
  - Support for quality-of-service (QoS)
- Differential SyncBus for synchronous operation with multiple RTD DSPs and data acquisition modules
  - Allows simultaneous sampling between multiple boards
  - Allows multiple boards to share a common clock
  - Allows synchronization of the sampling clock on multiple boards
  - Allows synchronization of start and stop triggers on multiple boards
  - Software selectable termination
  - Can be cabled or stacked
- Serial Port (RS-232/422/485)
- General Purpose I/O
  - 14-bit port of digital I/O
  - Bit-programmable direction
  - 5V Tolerant 3VTTL signaling level
- Programming modes
  - JTAG connector for programmer / emulator with Code Composer Studio
  - With a CPU over the PCIe/104 connector
- Additional Hardware Features
  - Status LED
  - Reset Button Input
- -40 to +85C standard operating temperature
- Heatsink Options
  - Thermal-optimized mini-fan heatsink included (standard)
  - Modified heatsinks and flat heatspreaders are available
  - Passive Structural Heatsink & Heatpipes in IDAN and HiDAN System Configurations
- Power requirements: +5 V only

1.3 Ordering Information

1.3.1 SPM34CP and SPM35CP Model Options

The SPM34CP and SPM35CP are available with the following options:

Table 1: Ordering Options

(IDAN) - **S P M 3** (B) **C P** (Nxxxx) **H R –** (M) (F) **–** (S)	
Coding	**Description**
IDAN	Board option: - [blank] = Stand-alone board - IDAN = Stackable IDAN frame
B	Bus: - 4 = PCIe/104 Type 2 connector (utilizes x2 link) - 5 = PCIe/104 Universal connector (utilizes x1 link)
Nxxxxx	Processor frequency and number of cores - D1250 = Dual Core, 1250 MHz - E1250 = Octal Core, 1250 MHz
M	DDR3 Memory configuration - 2048 = 2048 MB with ECC - 4096 = 4096 MB with ECC
F	Heatsink options: - [blank] = Fan heatsink (see figure on page 15) - F = Flat heat-spreader (see figure on page 15) o *Not available on IDAN-SPM34CP*
S	SyncBus connector (CN11) options: - [blank] = Right-angle SyncBus header - SS = Stack-down SyncBus header

Many ordering configurations are available. A few example ordering numbers are shown in the table below:

Table 2: Example Part Numbers

Part Numbers	Description
SPM34CPD1250HR-2048 SPM35CPD1250HR-2048	Dual core DSP with 2048 MB memory and standard Fan Heatsink
SPM34CPE1250HR-4096 SPM35CPE1250HR-4096	Octal core DSP with 4086 MB memory and standard Fan Heatsink
SPM34CPE1250HR-4096F SPM35CPE1250HR-4096F	DSP with Flat heat-spreader
IDAN-SPM34CPE1250HR-4096 IDAN-SPM35CPE1250HR-4096	Octal core DSP with 4096 MB memory in a stackable IDAN configuration
IDAN-SPM34CPE1250HR-4096-SS IDAN-SPM35CPE1250HR-4096-SS	IDAN configuration with a Stack-down SyncBus header

The Intelligent Data Acquisition Node (IDAN™) building block can be used in just about any combination with other IDAN building blocks to create a simple but rugged 104™ stack. This module can also be incorporated in a custom-built RTD HiDAN™ or HiDANplus High Reliability Intelligent Data Acquisition Node. Contact RTD sales for more information on our high reliability systems.

1.3.2 CABLE KITS AND RECOMMENDED ACCESSORIES

XK-CM121 Cable Kit

For maximum flexibility, RTD provides a cable kit which may be purchased as an accessory for the SPM3xCP DSP module (ordering part number XK-CM121), which contains:

- One Digital I/O cable (16-pin 0.1" DIL socket connector to 25-pin D-sub female)
- One serial port cable (10-pin 0.1" DIL socket connector to 9-pin D-sub male)
- Two Ethernet cables (DIL-10 10-pin 0.1" DIL socket connector to RJ-45)

JTAG Emulator

The JTAG Emulator and Programming Connector (CN4) on the SPM3xCP is compatible with +1.8 V JTAG emulator hardware supplied by several manufacturers, including the Texas Instruments XDS100v2 JTAG Emulator.

1.3.1 PACKAGE CONTENTS

When you order the SPM3xCP dspModule, you will receive:

- The SPM3xCP dspModule
- Depending upon the model ordered, a fan heatsink or passive flat heat-spreader will be mounted to the SPM3xCP
- A companion CD containing this user's manual and the following software:
  - DSP platform library which provides routines for low-level DSP hardware initialization
  - Network Development Kit (NDK) for Ethernet communication
  - Boot Loader for standalone operation (boot from SPI Flash)
  - Linux software for communication and control of the DSP from a cpuModule
- A packet containing four 22mm spacing standoffs, four 0.6" spacing standoffs, standoff nuts and screws, and several jumpers

When you order the IDAN-SPM3xCP, you will also receive two RJ-45 jack adapters which adapt to the two 9-pin D (male) Ethernet connections on the back panel.

Figure 1: SPM34CPE1250HR-4096 with Fan Heatsink

1.4 Contact Information

1.4.1 Sales Support

For sales inquiries, you can contact RTD Embedded Technologies sales via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: sales@rtd.com

1.4.2 Technical Support

If you are having problems with your system, please try the steps in the Troubleshooting section of this manual.

For help with this product, or any other product made by RTD, you can contact RTD Embedded Technologies technical support via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: techsupport@rtd.com

2 Specifications

2.1 Operating Conditions

Table 3: Operating Environment and Storage Conditions

Symbol	Parameter	Test Condition	Min	Max	Unit
T_a	Operating Temperature		-40	+85	C
T_s	Storage Temperature		-55	+125	C
RH	Relative Humidity	Non-Condensing	0	90%	%
MTBF	Mean Time Before Failure (Telcordia Issue 2, Ground benign, controlled)	SPM34CP; 30°C; excludes fan		1,211,643	Hours
		SPM35CP; 30°C; excludes fan		1,288,071	Hours

2.2 Electrical Characteristics

The bus connectors on the SPM3xCP offer several voltage inputs. Only +5 V is required for operation, and is used to generate the voltage requirements for all onboard circuitry, including power pins on all external I/O connectors. All other bus connector supply voltages are pass-through from other modules and are not required for operation of the SPM3xCP.

Table 4: Supply Voltage Requirements

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{cc5}	5 V Supply Voltage		4.75	5.25	V
$V_{cc5\text{-}STBY}$	5 V Stand-by Supply Voltage		n/a	n/a	V
V_{cc3}	3.3 V Supply Voltage		n/a	n/a	V
V_{cc12}	12 V Supply Voltage		n/a	n/a	V
$V_{cc\text{-}12}$	-12 V Supply Voltage		n/a	n/a	V

Table 5: Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
P	Power Consumption	V_{cc5} = 5.0V SPM3xCPD1250HR-2048 SPM3xCPE1250HR-2048 SPM3xCPD1250HR-4096 SPM3xCPE1250HR-4096		 7 10 9.5 12.5	W
I_{cc5}	5V Input Supply Current	Typical Power SPM3xCPD1250HR-2048 SPM3xCPE1250HR-2048 SPM3xCPD1250HR-4096 SPM3xCPE1250HR-4096		 1.4 2.0 1.9 2.5	A
PCIe/104 Bus					
	Differential Output Voltage		0.8	1.2	V
	DC Differential TX Impedance		80	120	Ω
	Differential Input Voltage		0.175	1.2	V
	DC Differential RX Impedance		80	120	Ω
	Electrical Idle Detect Threshold		65	175	mV
Utility Connector (CN5)					
$I_{UTILVCC}$	Utility Supply Current			500	mA
General Purpose I/O (CN6)					
V_{OH}	Output Voltage High	I_{OH} = -4.0 mA	2.4	3.3	V
V_{OL}	Output Voltage Low	I_{OL} = 8.0 mA	0.0	0.4	V
V_{IH}	Input Voltage High		2.0	5.5	V
V_{IL}	Input Voltage Low		-0.5	0.8	V
$I_{ADIOVCC}$	Supply Current			500	mA

Table 5: Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
Serial Port (CN7), RS-232 Mode					
V_{OH}	Output Voltage High	R_L = 3 k Ohm	5.0	7.0	V
V_{OL}	Output Voltage Low	R_L = 3 k Ohm	-7.0	-5.0	V
V_{IH}	Input Voltage High		2.0	15	V
V_{IL}	Input Voltage Low		-15	0.6	V
Serial Port (CN7), RS-422/485 Modes					
V_{OD1}	Differential Output	R_L = 100 Ohm	2.0		V
V_{OD2}	Differential Output	R_L = 54 Ohm	1.5		V
V_{OC}	Common Mode Output	R_L = 54 or 100 Ohm		3.0	V
V_{TH}	Differential Input Threshold		-200	-50	mV
V_I	Absolute Max Input Voltage		-18	18	V
SyncBus, LVDS (CN11)					
	Differential Input Voltage			2.4	V
	Input Voltage Threshold		-0.05	0.05	V
	Differential Output Voltage	I_O = -4µA	0.480	0.650	V
	Common Mode Output Voltage	I_O =-20µA	0.3	2.1	V
Fan Power Connector (CN15)					
I_{FAN}	Input Current to Fan			200	mA

2.3 Physical Characteristics

STEP models for the SPM34CP and SPM35CP are available upon request. Contact RTD Technical Support for more information.

- Weight: Approximately 0.18 kg (0.40 lbs.)
- Dimensions: 90.17 mm L x 95.89 mm W (3.550 in L x 3.775 in W)

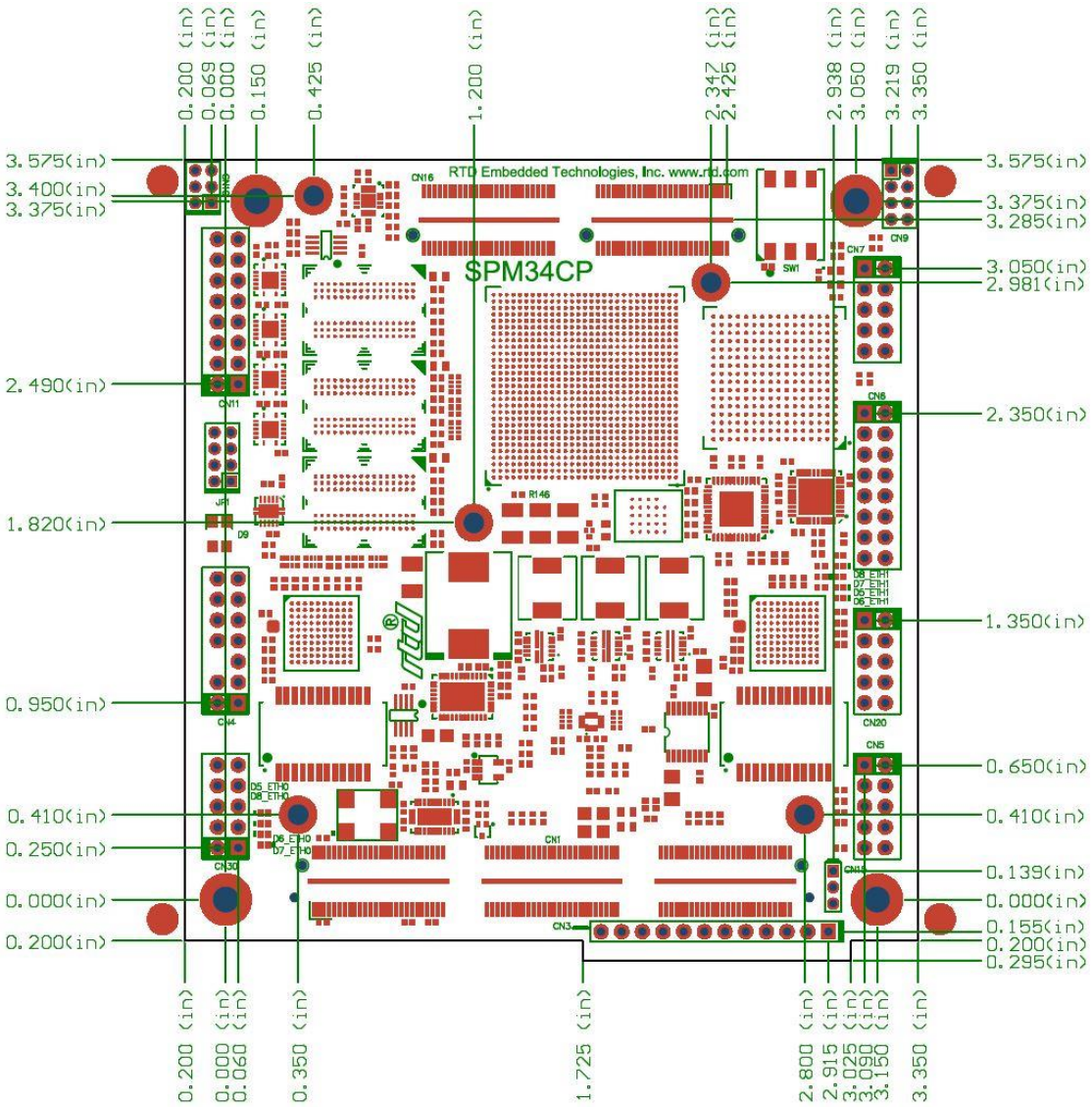


Figure 2: Board Dimensions

2.3.1 HEATSINK DIMENSIONS

The figures below show the thermally optimized fan heatsink and passive flat heat-spreader designed for the SPM3xCP dspModule. The heatsink option which is installed on the SPM3xCP at the factory is dictated by the ordering options shown on page 9.

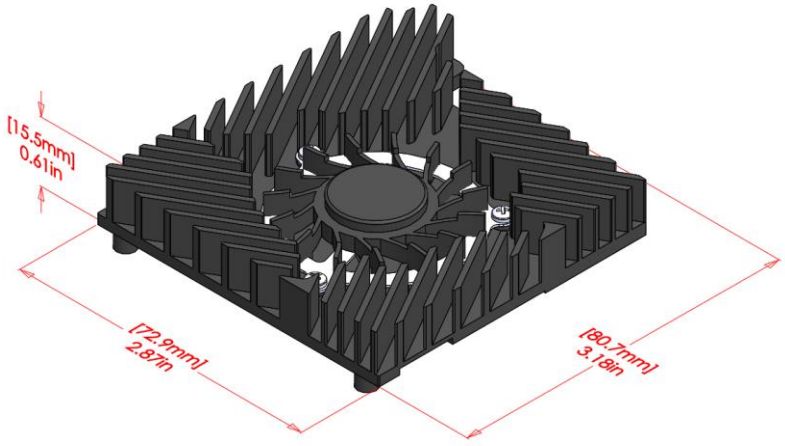


Figure 3: Fan Heatsink Dimensions

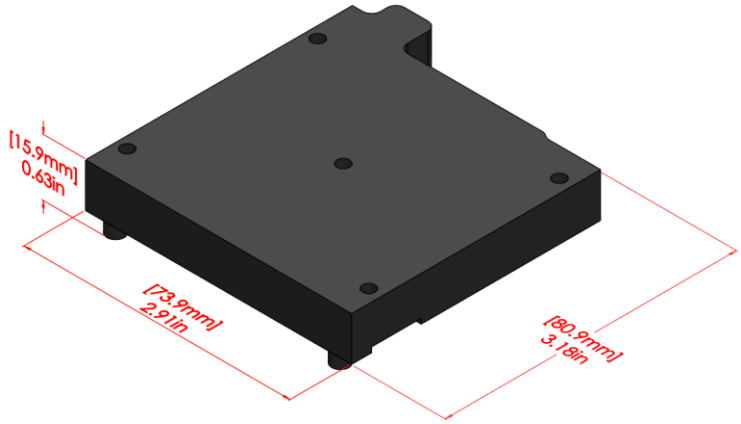


Figure 4: Flat Heat-Spreader Dimensions

3 Board Connections

3.1 Board Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your board in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the board at the edges, and do not touch the components or connectors. Handle the board in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

3.2 Steps for Installing

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the PC/104 system or stack.
3. Select and install stand-offs to properly position the module on the stack.
4. Remove the module from its anti-static bag.
5. Check that pins of the bus connector are properly positioned.
6. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
7. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
8. Gently and evenly press the module onto the PC/104 stack.
9. If any boards are to be stacked above this module, install them.
10. Attach any necessary cables to the PC/104 stack.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

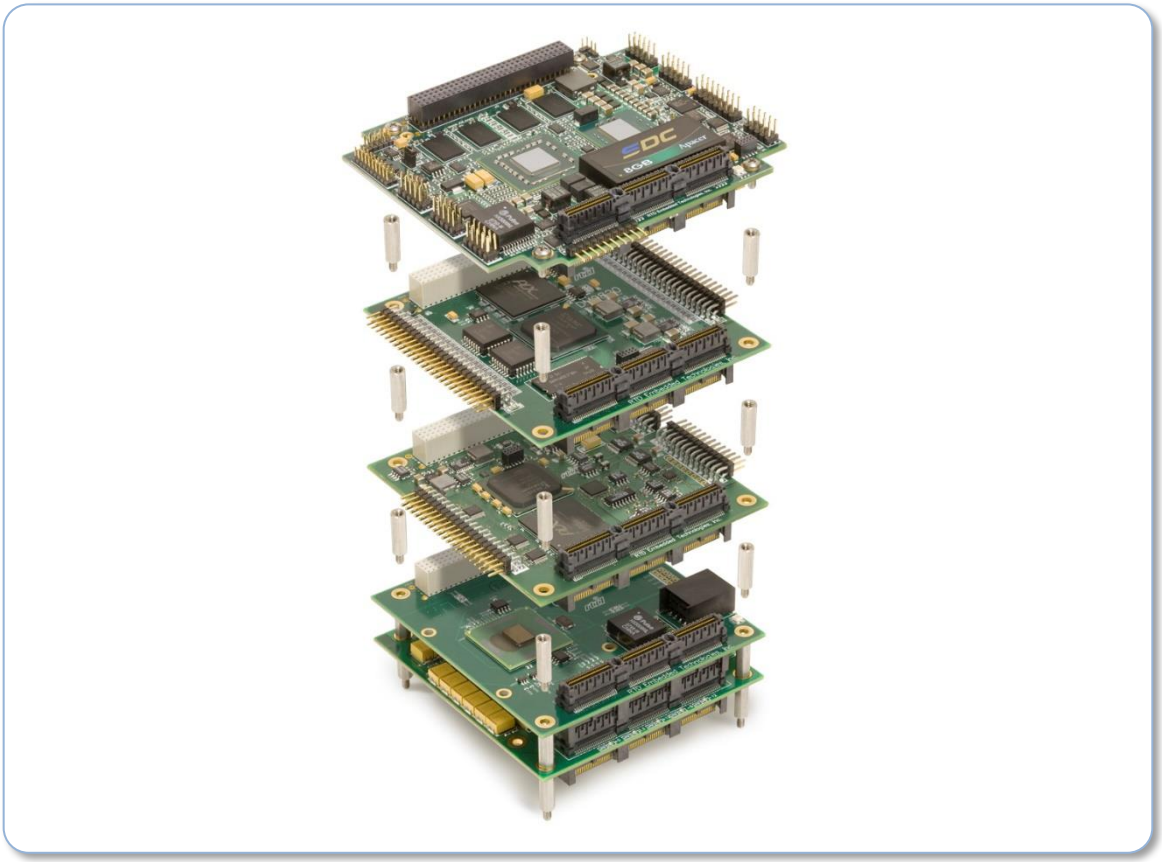


Figure 5: Example 104™ Stack

3.3 Applying Power for the First Time

The SPM3xCP does not support ATX power supply signaling. Therefore, if the DSP is not used with an ATX-compatible CPU, you will need to disable ATX signaling on the power supply or the DSP will not boot. This can usually be accomplished by closing a physical jumper or solder jumper on the power supply module. Consult the manual of your ATX power supply for more information.

When the SPM3xCP is used with a CPU which does support ATX signaling, the PCIe/104 power supply may be used in ATX mode, as the CPU will handle turning the supply on during the system's power-on sequence.

3.4 Connectors and Jumper Locations

The tables in this section list designator callouts for the various functions of the bus connectors, I/O connectors, and jumpers found on the SPM3xCP. Also included are the size and pitch of each connector as well as mating connector information. The following top-side photo provides a reference for designators and their locations.

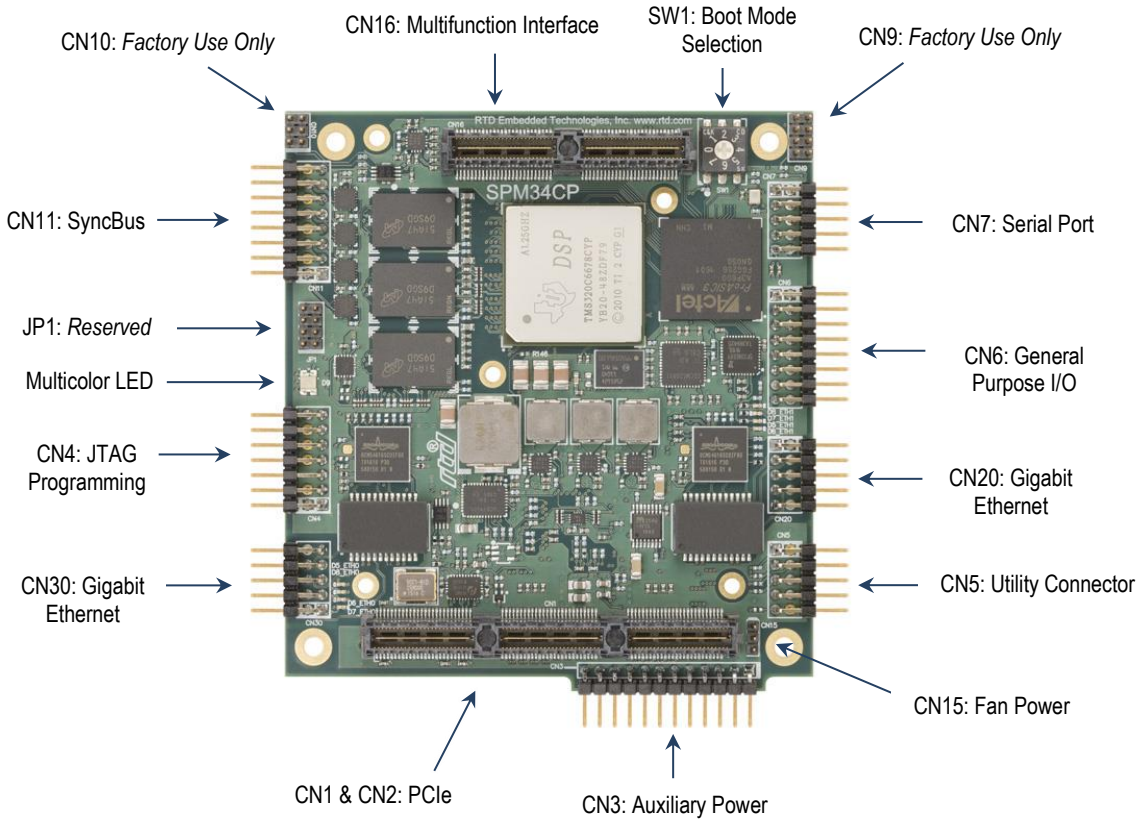


Figure 6: Board Connections

3.5 Connector and Jumper Functionality

3.5.1 Bus Connectors

Connectors CN1 and CN2 allow the DSP to connect it to a host cpuModule to be used as a DSP co-processor or accelerator. When the operating mode of the SPM3xCP is configured for stand-alone mode, the connectors also provide a robust connection to power the board.

Connector CN16 is the Multifunction Interface, and provides four high-speed Serial RapidIO® connections for robust system-level peer-to-peer data transfer. The connector also provides access to the SyncBus, permitting connected peripherals to be synchronized by the DSP. A SPI bus with four chip selects completes the connector.

Table 6: SPM3xCP Bus Connectors

Connector	Function	Location	Size and Pitch	Mating Connector
CN1	PCIe/104 Bus	Top	156-pin, 0.635mm	Samtec ASP-129646-03
CN2	PCIe/104 Bus	Bottom	156-pin, 0.635mm	Samtec ASP-129637-03
CN16	Multifunction Interface	Top	104-pin, 0.635mm	Samtec ASP-129646-02

The SPM3xCP is not configured to host PCIe peripherals. The PCIe connections on the PCIe/104 bus connectors are provided so the DSP can be configured as a peripheral to the host cpuModule.

PCIe Connectors (CN1 – Top, CN2 – Bottom)

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 47)

The SPM34CP is a Type 2 board, and can only connect to Type 2 PCIe/104 connector.

The SPM35CP uses universal PCIe/104 connections, and may be connected to Type 1 or Type 2 PCIe/104 connectors.

Multifunction Interface (CN16)

The Multifunction Interface (CN16) offers four lanes of Serial RapidIO®, a stackable SyncBus to synchronize simultaneously sampling DAQ cards with the DSP, and a SPI bus with four chip selects.

Table 7: Multifunction Interface (CN16) Pinout

Pin Name	#	#	#	Pin Name
GND	1		1	GND
sRIO_TD0p	3		3	sRIO_TD1p
sRIO_TD0n	5		5	sRIO_TD1n
GND	7		7	GND
sRIO_TD3p	9		9	sRIO_TD2p
sRIO_TD3n	11		11	sRIO_TD2n
GND	13		13	GND
sRIO_RD0p	15		15	sRIO_RD1p
sRIO_RD0n	17		17	sRIO_RD1n
GND	19		19	GND
sRIO_RD3p	21		21	sRIO_RD2p
sRIO_RD3n	23		23	sRIO_RD2n
GND	25	+5 V	25	GND
Reserved	27		27	*Reserved*
Reserved	29		29	*Reserved*
GND	31		31	GND
Reserved	33		33	*Reserved*
Reserved	35		35	*Reserved*
GND	37		37	GND
Reserved	39		39	*Reserved*
Reserved	41		41	*Reserved*
GND	43		43	GND
Reserved	45		45	*Reserved*
Reserved	47		47	*Reserved*
GND	49		49	GND
Reserved	51		51	*Reserved*
Pin Name	**#**	**#**	**#**	**Pin Name**
GND	53		53	GND
sRIO_0CLKp	55		55	sRIO_1CLKp
sRIO_0CLKn	57		57	sRIO_1CLKn
GND	59		59	GND
sRIO_3CLKp	61		61	sRIO_2CLKp
sRIO_3CLKn	63		63	sRIO_2CLKn
GND	65		65	GND
Reserved	67		67	*Reserved*
Reserved	69		69	*Reserved*
GND	71		71	GND
Reserved	73		73	*Reserved*
Reserved	75		75	*Reserved*
GND	77	+12 V	77	GND
SYNC0p	79		79	SYNC1p
SYNC0n	81		81	SYNC1n
GND	83		83	GND
SYNC3p	85		85	SYNC2p
SYNC3n	87		87	SYNC2n
GND	89		89	GND
SPI_CS0#	91		91	SPI_CS1#
SPI_CS3#	93		93	SPI_CS2#
GND	95		95	GND
SPI_DO	97		97	SPI_DI
GND	99		99	GND
RESET#	101		101	SPI_CLK
DIR (GND)	103		103	GND

Serial RapidIO®

For instructions on how to use the Serial RapidIO connections on the SPM3xCP, refer to page 35.

Stackable SyncBus

For instructions on how to use the SyncBus, refer to page 35.

SPI Bus

For instructions on how to use the SPI connections of the Multifunction Interface (CN16), refer to page 36.

3.5.2 External I/O Connectors

For all connectors, pin 1 is designated by a thick white silkscreen line, and a square pad on the PCB.

Table 8: SPM3xCP External I/O and Mating Connectors

Designator	Function	Size and Pitch	Mating Connector
CN3	Auxiliary Power Input	1x12, 0.1", right angle	FCI 65039-025LF
CN4	JTAG Connector	2x7, 0.1", right angle	3M 89114-0001
CN5	Utility Connector	2x5, 0.1", right angle	3M 89110-0001
CN6	General Purpose I/O	2x13, 0.1", right angle	3M 89116-0001
CN7	Serial Port	2x5, 0.1", right angle	3M 89110-0001
CN11	SyncBus	1x8, 0.1", right angle	3M 89116-0001
CN20	Gigabit Ethernet	2x5, 0.1", right angle	3M 89110-0001
CN30	Gigabit Ethernet	2x5, 0.1", right angle	3M 89110-0001
CN9	*Factory Use Only*	2x5, 2mm, vertical	—
CN10	*Factory Use Only*	2x3, 2mm, vertical	—

Auxiliary Power Connector (CN3)

RTD generally advises against powering the board through CN3, and instead recommends that input power is applied to the SPM3xCP through the PCIe/104 connectors (CN1 or CN2). This is especially true when multiple boards are being powered in a stack, where the input connections may not be suitable for high power conditions.

For lower power DSP applications where true stand-alone operation is desired, the Auxiliary Power Connector (CN3) provides an alternate option to powering the module through one of the PCIe/104 connectors. Only +5 V is required for operation.

Follow these guidelines when connecting a power source to the auxiliary power connector:

1. Use short wires when possible.
2. Power must be provided on each +5 V pin, with ground connections made to each neighboring +5 V pin.
3. Twist wires connecting adjacent +5 V and GND pins between the power supply and the connector to reduce noise induced onto the wires from external sources.
4. When power is applied, the voltage as measured at the connector must be +5 V nominal.

Table 9 provides the pin connections for the Auxiliary Power Connector:

Table 9: Auxiliary Power Connector (CN3) Pinout

12	11	10	9	8	7	6	5	4	3	2	1
GND	+5 V	+5 V	GND	GND	*Reserved*		GND	GND	+5 V	+5 V	GND

JTAG Emulator and Programming Connector (CN4)

The JTAG Emulator and Programming Connector (CN4) on the SPM3xCP is used for programming firmware to the DSP from TI's Code Composer Studio. The connector is compatible with +1.8 V JTAG emulator hardware supplied by several manufacturers, including the Texas Instruments XDS100v2 JTAG Emulator.

Table 10: JTAG Connector (CN4) Pinout

TMS	1	2	TRST
TDI	3	4	GND
+1.8 V	5	6	(Key)
TDO	7	8	GND
RTCK	9	10	GND
TCK	11	12	GND
EMU0	13	14	EMU1

Facing the JTAG Programming Connector, the pinout is:

13	11	9	7	5	3	1
EMU0	TCK	RTCK	TDO	+1.8 V	TDI	TMS
EMU1	GND	GND	GND	(Key)	GND	TRST
14	12	10	8	6	4	2

Utility Connector (CN5)

The Utility Connector (CN5) implements a manual push-button reset input, LED connections, and a +5 V current limited power output. The LED and +5V_UTIL output may be configured by the LED_COLOR and UTIL_PWR_EN registers (page 39).

Table 11: Utility Connector (CN5) Pinout

Pin	Signal	Function	In/Out
1	RESET#	Manual Push-Button Reset	in
2	GND	Ground	—
3	LED_RED	Multi-color LED, Red Component	out
4	LED_GREEN	Multi-color LED, Green Component	out
5	LED_BLUE	Multi-color LED, Blue Component	out
6	+5V_UTIL	+5 V, Current Limited	out
7	*Reserved*	—	—
8	*Reserved*	—	—
9	*Reserved*	—	—
10	GND	Ground	—

Facing the Utility Connector, the pinout is:

9	7	5	3	1
Reserved	*Reserved*	LED_BLUE	LED_RED	RESET#
GND	*Reserved*	+5V_UTIL	LED_GREEN	GND
10	8	6	4	2

The RESET# Input

Asserting the push-button reset will assert the RESETFULL pin on the TI DSP (an active low input). The will issue a Power On Reset (POR) to the DSP, resulting in a total reset of the DSP chip to its default state, as well as a reset to all DSP test and emulator logic. Additionally, the boot mode of the DSP will be re-latched, and the boot process will be reinitiated. For more information on the DSP chip's RESETFULL pin, refer to the Texas Instruments documentation.

NOTE: It is recommended that the RESET# input is not used when the SPM3xCP is connected as a peripheral to a host cpuModule, as asserting the RESET# input will result in the SPM3xCP disappearing from PCI device space.

Asserting the RESET# input on the Utility Connector (CN5) will result in resetting all registers on the TI C6678's EMIF16 interface to their default state. (A full description of the board registers begins on page 37.)

General Purpose I/O (CN6)

Connector CN6 provides access to the DSP's General Purpose I/O pins, GP[13:0].

To configure the direction of a pin, the corresponding bit of the GPIO_DIRECTION register must be set. This must coincide with setting the direction of the GP[13:0] pins of the DSP, and must carefully take into consideration the order of which each device pin's direction is set. Details on setting the GPIO_DIRECTION register are discussed on page 38.

Table 12: GPIO Connector (CN6) Pinout

GPIO(0)	1	2	GPIO(1)
GPIO(2)	3	4	GPIO(3)
GPIO(4)	5	6	GPIO(5)
GPIO(6)	7	8	GPIO(7)
GPIO(8)	9	10	GPIO(9)
GPIO(10)	11	12	GPIO(11)
GPIO(12)	13	14	GPIO(13)
GND	15	16	+5V_GPIO

The +5V_GPIO output (pin 16) is turned ON by default, but may be toggled ON/OFF using the GPIO_PWR_EN register (page 38).

Serial Port (CN7)

The SPM3xCP serial port connector (CN7) connects to a UART in the TI DSP chip. The onboard transceiver supports RS-232/422/485 modes, and may configured using the FPGA's SER_PORT_CTRL register (page 43).

Table 13 provides the serial port connector pinout when RS-232 mode is enabled:

Table 13: Serial Port (CN7) in RS-232 Mode

DIL Pin	Signal	Function	In/Out	DB-25	DB-9
1	—	*Reserved*	—	8	1
2	—	*Reserved*	—	6	6
3	RXD	Receive Data	In	3	2
4	RTS	Request To Send	out	4	7
5	TXD	Transmit Data	out	2	3
6	CTS	Clear To Send	in	5	8
7	—	*Reserved*	—	20	4
8	—	*Reserved*	—	22	9
9	GND	Signal Ground	—	7	5
10	GND	Signal Ground	—	—	—

Facing the serial port connector, the pinout in RS-232 mode is:

9	7	5	3	1
GND	—	TXD	RXD	—
GND	—	CTS	RTS	—
10	8	6	4	2

Table 14 provides the serial port connector pinout when RS-422 mode is enabled:

Table 14: Serial Port (CN7) in RS-422 Mode

DIL Pin	Signal	Function	In/Out	DB-25	DB-9
1	TXD-	Transmit Data (-)	out	8	1
2	—	*Reserved*	—	6	6
3	TXD+	Transmit Data (+)	out	3	2
4	—	*Reserved*	—	4	7
5	RXD+	Receive Data (+)	in	2	3
6	—	*Reserved*	—	5	8
7	RXD-	Receive Data (-)	in	20	4
8	—	*Reserved*	—	22	9
9	GND	Signal Ground	—	7	5
10	GND	Signal Ground	—	—	—

Facing the serial port connector, the pinout in RS-422 mode is:

9	7	5	3	1
GND	RXD-	RXD+	TXD+	TXD-
GND	—	—	—	—
10	8	6	4	2

Table 15 provides the serial port connector pinout when RS-485 mode is enabled:

Table 15: Serial Port (CN7) in RS-485 Mode

DIL Pin	Signal	Function	In/Out	DB-25	DB-9
1	D-	Data (-)	in/out	8	1
2	—	*Reserved*	—	6	6
3	D+	Data (+)	in/out	3	2
4	—	*Reserved*	—	4	7
5	—	*Reserved*	—	2	3
6	—	*Reserved*	—	5	8
7	—	*Reserved*	—	20	4
8	—	*Reserved*	—	22	9
9	GND	Signal Ground	—	7	5
10	GND	Signal Ground	—	—	—

Facing the serial port connector, the pinout in RS-485 mode is:

9	7	5	3	1
GND	—	—	D+	D-
GND	—	—	—	—
10	8	6	4	2

SyncBus (CN11)

The SyncBus Connector is a 2 x 8, 0.1" spacing right-angle connector. The pin assignments are shown in Table 16 below. Details on using the SyncBus are described on page 35.

Table 16: SyncBus Connector (CN11) Pinout

SYNC0p	1	2	SYNC0n
GND	3	4	GND
SYNC1p	5	6	SYNC1n
GND	7	8	GND
SYNC2p	9	10	SYNC2n
GND	11	12	GND
SYNC3p	13	14	SYNC3n
GND	15	16	GND

Gigabit Ethernet (CN20 & CN30)

Connectors CN20 and CN30 provide a switched connection to a single Gigabit Ethernet controller within the DSP, permitting the controller to be physically connected to two devices in a system. The Gigabit Ethernet controller supports 10Base-T and 100BaseTX in half- or full-duplex mode, and 1000BaseT in full-duplex mode, with hardware flow control and support for quality-of-service (QOS).

For configuration details on the DSP's Gigabit Ethernet Switched Subsystem, refer to the Texas Instruments documentation.

Table 15 provides the pinout for the Gigabit Ethernet connectors:

Table 17: Gigabit Ethernet (CN20 & CN30) Connector Pinout

DIL Pin	Signal	Function	RJ-45 Pin
1	B+ (RX+)	Receive+ (10/100)	3
2	B- (RX-)	Receive- (10/100)	6
3	C+		4
4	C-		5
5	A+ (TX+)	Transmit+ (10/100)	1
6	A- (TX-)	Transmit- (10/100)	2
7	D+		7
8	D-		8
9	AGND	Ethernet Ground	—
10	AGND	Ethernet Ground	—

Facing the connector, the pinout for Gigabit Ethernet is:

9	7	5	3	1
AGND	D+	A+ (TX+)	C+	B+ (RX+)
AGND	D-	A- (TX-)	C-	B- (RX-)
10	8	6	4	2

Fan Power Connector (CN15)

The pinout for the Fan Power Connector (CN15) is shown in Table 18.

Table 18: Fan Power Connector (CN15) Pinout

Pin	Signal	Function
1	+5 V	Fan power
2	GND	Ground
3	*Reserved*	

Factory Use Only (CN9 & CN10)

Headers CN9 and CN10 are for factory use only.

3.5.3 BOOT SELECTOR SWITCH (SW1)

To select the boot mode of the DSP, set the position of the Boot Selector Switch (SW1) to the numeric position in Table 19 that corresponds to the boot mode. Detailed information on the supported boot modes is described on page 33.

Table 19: Selectable Boot Devices

Switch Position (SW1)	Boot Mode
0	PCIe Boot (requires a host cpuModule)
1	Boot to SPI Flash with starting address 0x00100000 (64k)
2	Boot to SPI Flash with starting address 0x00400000 (4M)
3	Boot to SPI Flash with starting address 0x00800000 (8M)
4	Boot to SPI Flash with starting address 0x00C00000 (12M) *(This mode is pre-programmed at the factory. See below for more information.)*
5	Ethernet Boot
6	*Reserved*
7	*Reserved*

Boards will leave the factory with bootable DSP firmware programmed to 0x00C00000. This will allow the user to quickly see that their DSP is operational. To test, the boot selection switch should be moved to position 4 before power is applied. After applying power, the onboard LED will change to white, and repeatedly toggle on and off.

3.5.4 JUMPER BLOCK (JP1)

Jumper block (JP1) is reserved for future use.

4 IDAN Connections

4.1 Module Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your module in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the module by the aluminum enclosure, and do not touch the components or connectors. Handle the module in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

4.2 Physical Characteristics

- Weight: Approximately 0.86 kg (1.90 lbs.)
- Dimensions: 152 mm L x 168 mm W x 41 mm H (5.98 in L x 6.62 in W x 1.63 in H)

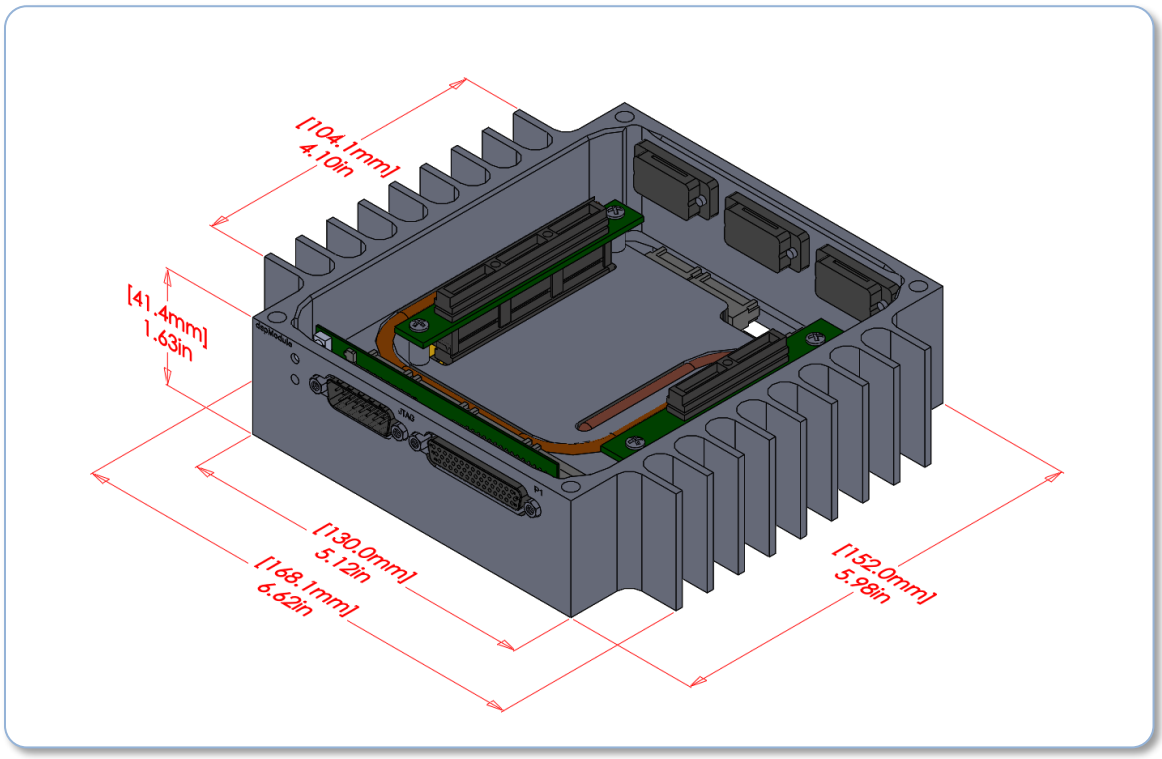


Figure 7: IDAN-SPM3xCP Dimensions

4.3 Connector Locations

The diagrams below show the connector locations for the headers of the SPM3xCP as they are brought out on the front and back panels of the IDAN-SPM3xCP. For a full description of each connector on the SPM3xCP, refer to the External I/O Connectors section of this manual on page 20.

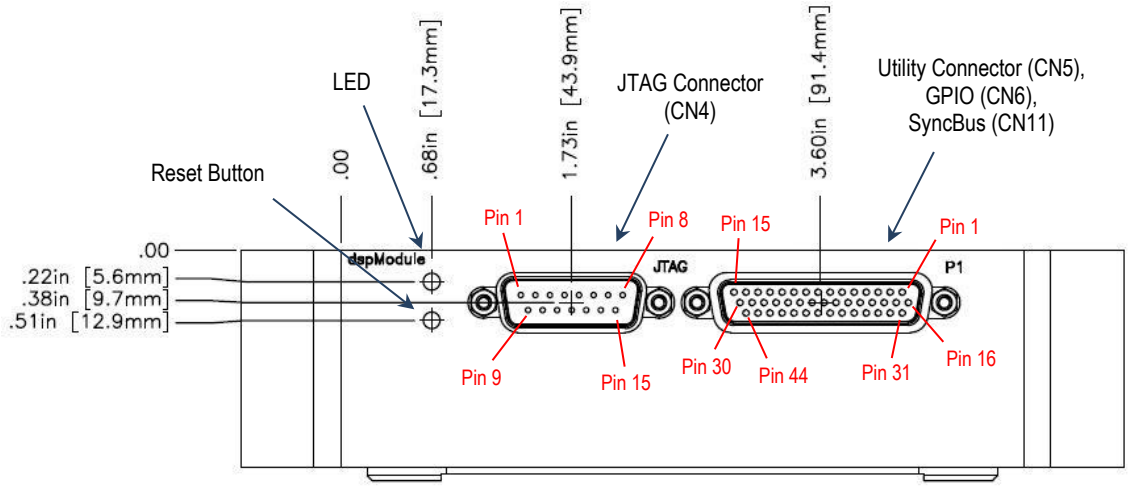


Figure 8: IDAN Front Panel Connectors

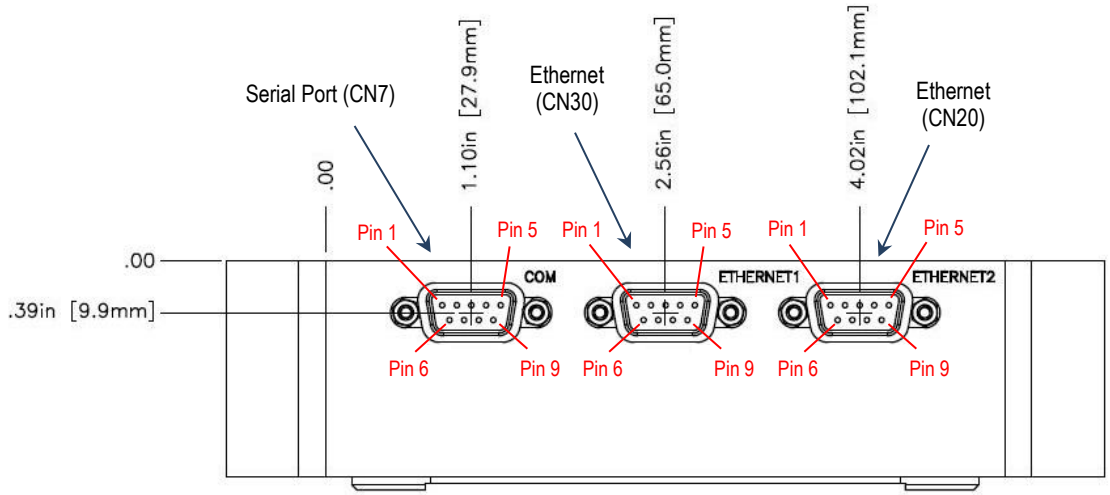


Figure 9: IDAN Back Panel Connectors

4.4 Connector Pinouts

The connector and pinouts for the IDAN-SPM3xCP front and back panels are described in the sections below.

Table 20: SPM3xCP External I/O and Mating Connectors

Designator	Function	Connector Description	IDAN Panel Connector	Example Mating Connector
CN4	JTAG Connector	15-pin D (male)	Nor Comp 171-015-113R011	AMP 747052-3
CN5	Utility Connector	44-pin HD (female)	Adam Tech HDT44STSL	AMP 5-747916-2
CN6	General Purpose I/O			
CN11	SyncBus			
CN7	Serial Port	9-pin D (male)	Adam Tech DE09PD	Adam Tech DE09SD
CN20	Gigabit Ethernet	9-pin D (male)	Adam Tech DE09PD	Adam Tech DE09SD
CN30	Gigabit Ethernet	9-pin D (male)	Adam Tech DE09PD	Adam Tech DE09SD

4.4.1 Panel LED and Reset Button

The LED on the IDAN-SPM3xCP front panel is a multi-color LED which connects directly to the LED_RED, LED_GREEN, and LED_BLUE outputs of the SPM3xCP's Utility Connector (CN5). The colors displayed by the LED will match that of the onboard surface-mount LED shown on the SPM3xCP board connections diagram (section 3.4). The colors of the LED are controlled by the LED_COLOR register (page 39).

The reset button is connected to the RESET# input on the SPM3xCP's Utility Connector (CN5), and drives the signal to GND when pushed.

4.4.2 JTAG Connector — 15-pin D Connector (male)

Table 21: IDAN JTAG Connector — 15-pin D Connector (male)

Pin # (15-D)	Signal	Function	In/Out	DIL Pin # (CN4)
1	TMS	JTAG Test Mode Input	in	1
2	TDI	JTAG Data Input	in	3
3	+1.8 V	+1.8 V Power	out	5
4	TDO	JTAG Data Output	out	7
5	RTCK	JTAG Clock Input (alternate)	in	9
6	TCK	JTAG Clock Input	in	11
7	EMU0	TI DSP Emulation Trace Port, pin EMU00	in/out	13
8	EMU1	TI DSP Emulation Trace Port, pin EMU01	in/out	14
9	TRST	JTAG Reset	in	2
10	GND	Ground	—	4
11	(Key)	Keying pin	—	6
12	GND	Ground	—	8
13	GND	Ground	—	10
14	GND	Ground	—	12
15	RSVD	*Reserved*	—	—

4.4.3 Gigabit Ethernet — 9-pin D Connector (male)

Table 22: IDAN Gigabit Ethernet — 9-pin D Connector (male)

Pin # (DIL)	Pin # (DB-9)	Signal	Function	Pin # (RJ-45)
1	1	B+ (RX+)	Receive+ (10/100)	3
2	6	B- (RX-)	Receive- (10/100)	6
3	2	C+		4
4	7	C-		5
5	3	A+ (TX+)	Transmit+ (10/100)	1
6	8	A- (TX-)	Transmit- (10/100)	2
7	4	D+		7
8	9	D-		8
9	5	AGND	Ethernet Ground	—
10	—	AGND	Ethernet Ground	—

4.4.4 Serial Port — 9-pin D Connector (male)

Table 23: IDAN Serial Port — 9-pin D connector (male)

Pin # (DIL)	Pin # (DB-9)	RS-232	RS-422	RS-485
1	1	—	TXD-	D-
2	6	—	—	—
3	2	RXD	TXD+	D+
4	7	RTS	—	—
5	3	TXD	RXD+	—
6	8	CTS	—	—
7	4	—	RXD-	—
8	9	—	—	—
9	5	GND	GND	GND
10	—	GND	GND	GND

4.4.5 MULTI-FUNCTION CONNECTOR — 44-PIN HIGH DENSITY "D" CONNECTOR (MALE)

The 44-pin High Density "D" connector contains pin connections to the SPM3xCP's Utility Connector (CN5), General Purpose I/O (CN6), and SyncBus (CN11).

Table 24: IDAN Multi-function Connector —44-Pin High Density "D" Connector (male)

Pin # (44-D)	Signal	Function	In/Out	DIL Pin # (CN5)	DIL Pin # (CN6)	DIL Pin # (CN11)
1	GND	Ground				
2	SYNC0p	SyncBus0p				1
3	GND	Ground				
4	SYNC1p	SyncBus1p				5
5	GND	Ground				
6	SYNC2p	SyncBus2p				9
7	GND	Ground				
8	SYNC3p	SyncBus3p				13
9	GND	Ground				
10	RESET#		in	1		
11	GND	Ground				
12	LED_RED	Multi-color LED, Red Component	out	3		
13	LED_GREEN	Multi-color LED, Green Component	out	4		
14	LED_BLUE	Multi-color LED, Blue Component	out	5		
15	+5V_UTIL	+5 V (Utility Connector), Current Limited	out	6		
16	GND	Ground				
17	SYNC0n	SyncBus0n				2
18	GND	Ground				
19	SYNC1n	SyncBus1n				6
20	GND	Ground				
21	SYNC2n	SyncBus2n				10
22	GND	Ground				
23	SYNC3n	SyncBus3n				14
24	GND	Ground				
25	GND	Ground				
26	GND	Ground				
27	*Reserved*	—		7		
28	*Reserved*	—		8		
29	*Reserved*	—		9		
30	+5V_GPIO	+5V (GPIO Connector), Current Limited	out		16	
31	GPIO(0)	GPIO(0)	in/out		1	
32	GPIO(1)	GPIO(1)	in/out		2	
33	GPIO(2)	GPIO(2)	in/out		3	
34	GPIO(3)	GPIO(3)	in/out		4	
35	GPIO(4)	GPIO(4)	in/out		5	
36	GPIO(5)	GPIO(5)	in/out		6	
37	GPIO(6)	GPIO(6)	in/out		7	
38	GPIO(7)	GPIO(7)	in/out		8	
39	GPIO(8)	GPIO(8)	in/out		9	
40	GPIO(9)	GPIO(9)	in/out		10	
41	GPIO(10)	GPIO(10)	in/out		11	
42	GPIO(11)	GPIO(11)	in/out		12	
43	GPIO(12)	GPIO(12)	in/out		13	
44	GPIO(13)	GPIO(13)	in/out		14	

4.5 Steps for Installing

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the IDAN system.
3. Remove the module from its anti-static bag.
4. Check that pins of the bus connector are properly positioned.
5. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
6. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
7. Gently and evenly press the module onto the IDAN system.
8. If any boards are to be stacked above this module, install them.
9. Finish assembling the IDAN stack by installing screws of an appropriate length.
10. Attach any necessary cables to the IDAN system.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

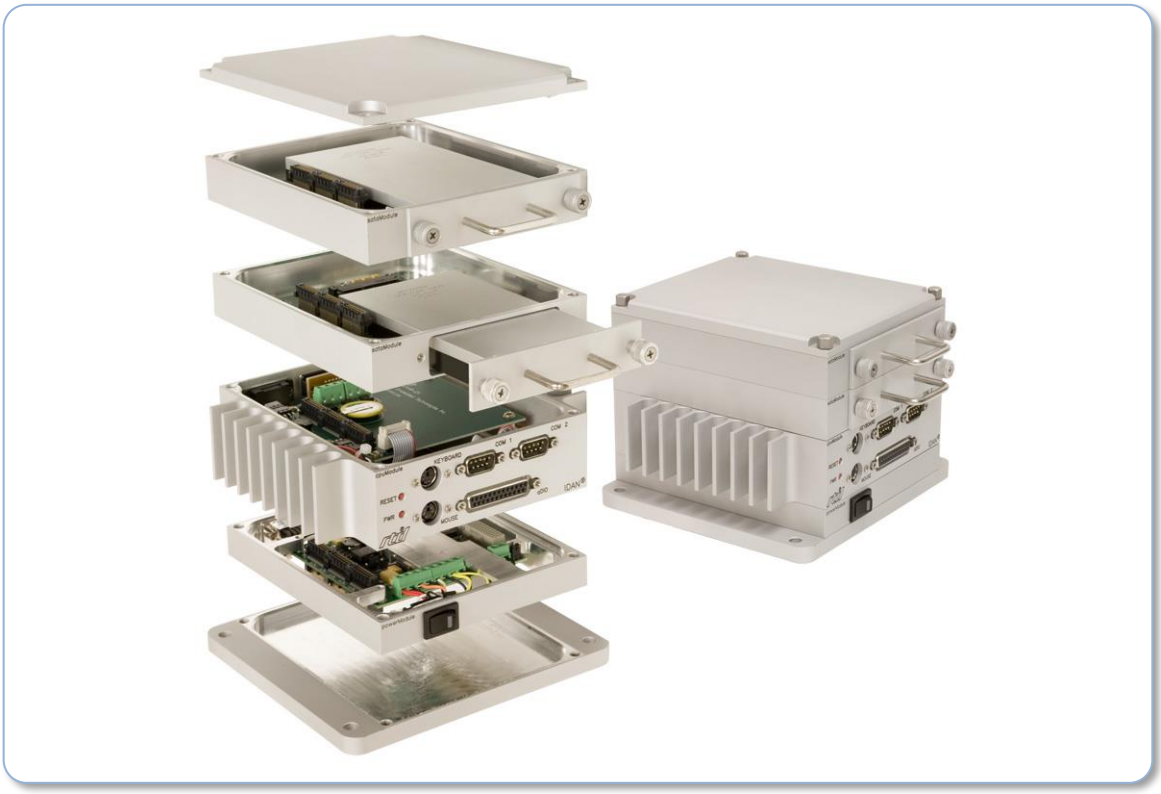


Figure 10: Example IDAN System

5 Functional Description

5.1 Functional Diagram

The figure below shows the functional diagram of the SPM3xCP. The various parts of the diagram are discussed in the following sections.

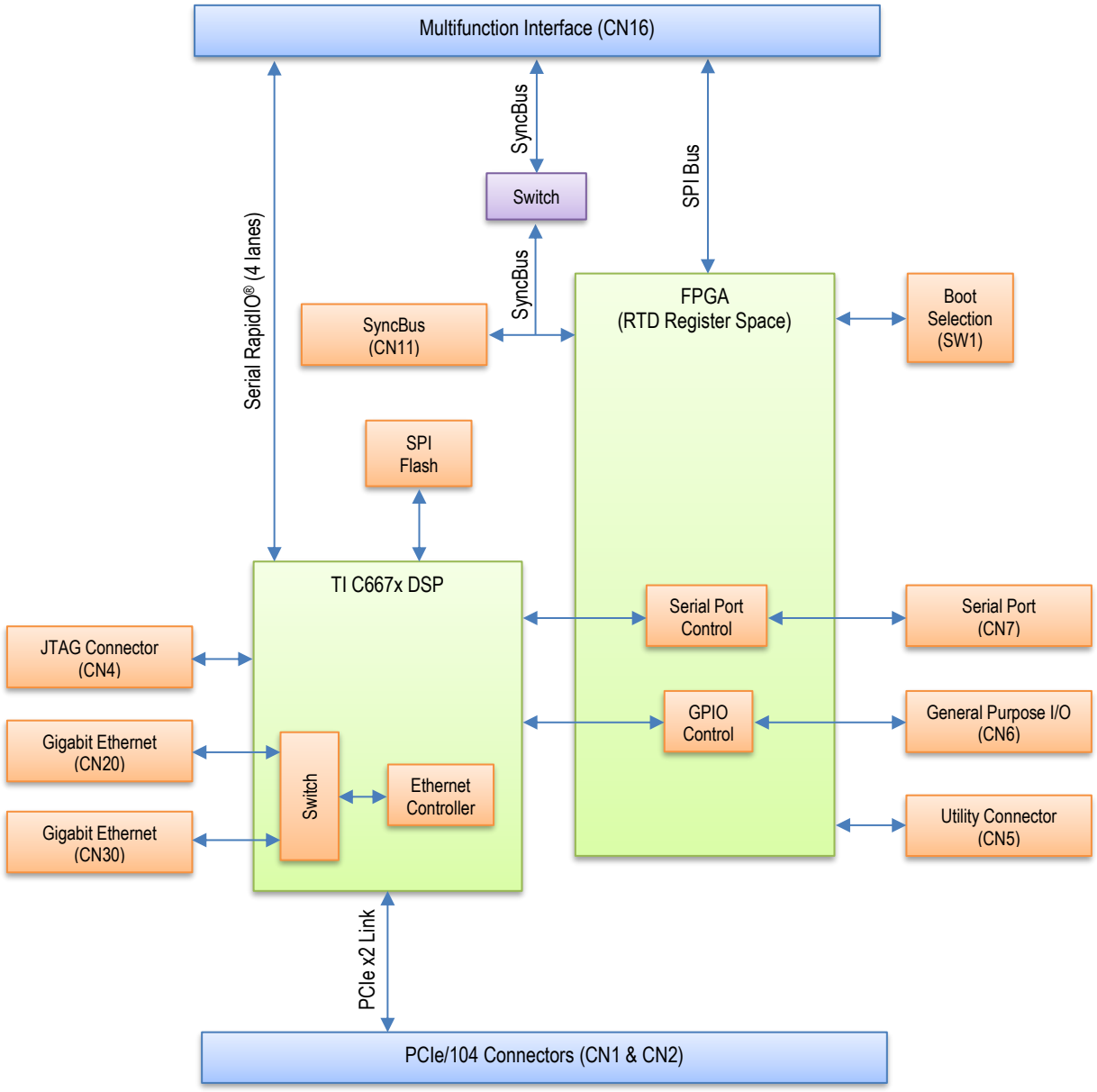


Figure 11: SPM34CP Functional Diagram

5.2 Operating Mode Selection

The SPM34CP supports multiple operating modes. Onboard flash permits true stand-alone operation of the DSP without a host or as a high-speed accelerator to an analog front-end module, while the PCI Express connector alternatively permits the DSP to act a co-processor to a PCIe/104 host cpuModules.

- The SPM34CP utilizes a PCIe x2 link for communication, which requires a PCIe/104 Type 2 connector to the host cpuModules
- The SPM35CP utilizes a PCIe x1 link for communication, permitting either a PCIe/104 Type 1 or Type 2 connection to the host cpuModules.

Booting to device over the Gigabit Ethernet connection is also supported.

To select the desired boot mode of the DSP, use the Boot Selection Switch (SW1), described on page 26.

5.2.1 Stand-Alone Operation

Boot to SPI Flash Memory

The SPM34CP provides 16MB of onboard SPI flash memory for storing bootable DSP firmware. The memory is separated into several sectors, four of which are used to store DSP programs which may be loaded and executed by the SPM34CP after power is applied.

To select which of the four sectors is loaded and executed at boot, the Boot Selection Switch (SW1) must be set to the position corresponding to the sector at which the desired DSP program is stored. Switch positions 1, 2, 3, and 4 point to the four different bootable sectors.

To load a Code Composer Studio *.out file to one of four sectors of the SPI flash, a special SPI writer utility must be used. This utility is packaged on the companion CD shipped with the SPM34CP.

The addressable space of the SPI flash is shown in the table below, along with the corresponding boot mode positions.

Table 25: SPI Flash Sectors

Sector Starting Address	Function
0x00000000	*Reserved (SPI Jump Table)*
0x00100000 (64k)	Configure Boot Selection Switch (SW1) to position 1 to boot from this address
0x00400000 (4MB)	Configure Boot Selection Switch (SW1) to position 2 to boot from this address
0x00800000 (8MB)	Configure Boot Selection Switch (SW1) to position 3 to boot from this address
0x00C00000 (12MB)	Configure Boot Selection Switch (SW1) to position 4 to boot from this address *(This mode is pre-programmed at the factory. See page 26 for more information.)*

While a host cpuModule is not required for these boot modes, a host is still permitted if required by the application.

WARNING: The SPI Jump Table should never be overwritten by the user. Doing so will break the SPI Flash boot modes enabled by the Boot Selection Switch (SW1). If the SPI Jump Table is accidentally overwritten, it must be rewritten using a special utility. This utility is packaged on the companion CD shipped with the SPM34CP.

Boot to Ethernet

The SPM34CP supports booting to Ethernet. For more information, consult the TI documentation for the TMS320C6678.

5.2.2 With a Host CPU

Boot to PCIe

RTD provides Linux software for communication and control of the DSP from a cpuModule. An example program is provided on the SPM34CP companion CD which demonstrates the steps of loading a program onto the DSP and beginning its execution.

5.3 Interrupts

5.3.1 Interrupts from the Host to the DSP

The Host is capable of sending a message signaled interrupt (MSI) directly to a C66x CorePac of the DSP. These interrupts can be handled inside the DSP by means of user-defined interrupt handler codes. An example program is provided on the SPM34CP companion CD which demonstrates sending and handling of Host to DSP interrupts.

5.3.2 Interrupts from the DSP to the Host

The DSP is capable of sending an interrupt request to the Host through the PCI-express bus. The Linux kernel driver provided on the SPM34CP companion CD is prepared to capture interrupts coming from the DSP. An example program demonstrating the usage of DSP to Host interrupts is also provided on the companion CD.

5.4 Serial RapidIO®

The SPM34CP module's Multifunction Interface (CN16) features four lanes of Serial RapidIO (SRIO), a high-bandwidth, system-level interconnect permitting high speed peer-to-peer data transfer between DAQ modules, FPGA modules, and DSP modules at gigabyte-per-second performance levels.

The principle features of Serial RapidIO include:

- Flexible system architecture that allows peer-to-peer communication
- Robust communication with error-detection features
- Frequency and port-width scalability
    - The SRIO ports on the SPM34CP's Multifunction Interface (CN16) can be configured as four x1, two x2, one x4, and two x1 + one x2
- Operation that is not software intensive
- High-bandwidth interconnect with low overhead
- Low latency
- Low power

For more information on how to use the Serial RapidIO on the SPM34CP's Multifunction Interface (CN16), consult the TI documentation for the TMS320C6678.

Additional resources for Serial RapidIO are listed in section 8.3.

5.5 SyncBus

The SPM34CP features an LVDS SyncBus which may be used on either the SyncBus I/O connector (CN11) or the Multifunction Interface (CN16).

The SyncBus provides the user with one 10MHz based master clock and three event based triggering outputs. To use any of the SyncBus lines the module must be configured to use the SyncBus master clock. An example program is provided on the SPM34CP companion CD which demonstrates how to use the SyncBus.

SYNC0p/n – SYNC2p/n may be used as output clocks or general purpose LVDS I/O. When configured as output clocks, they can output a divided down version of the 10MHz master clock using the SYNC_TICK_0, SYNC_TICK_1, and SYNC_TICK2 registers (page 42), which can be then used to trigger events on other modules in the system. To set the SYNC0p/n –SYNC2p/n pins as output clocks or GPIO, use the SYNC_MODE register (page 41).

SYNC3p/n may also be as an output clock or as a general purpose LVDS I/O. However, when configured to be a clock, SYNC3p/n is the master clock of the SyncBus. This clock is used to synchronize multiple boards featuring the LVDS SyncBus. To synchronize multiple boards, you must set one board as an output and the rest as inputs. On the board that is set as an output, the master will drive a 10MHz clock on SyncBus3 to synchronize all the boards set as inputs, or slaves. The SPM34CP is always configured as an output.

NOTE: Only enable one output per SyncBus line when synchronizing multiple boards. Enabling multiple outputs on a SyncBus line will result in unexpected behavior.

5.5.1 SyncBus Termination

Due to the multi-drop nature of the SyncBus, termination must be enabled on the boards which are the endpoints of the connection. For example, if three boards are stacked together -- *A*, *B*, and *C* – termination must be anbled on boards *A* and *C*.

SyncBus termination on the SPM34CP can be enabled or disabled using the SYNC_CTRL register (page 40).

5.5.2 SyncBus on the Multifunction Interface

The SyncBus transceivers are used to drive the SyncBus connections on both the SyncBus I/O connector (CN11) as well as the connections on the Multifunction Interface (CN16). However, only one of these connectors should be used at a time.

When using the SyncBus connections on the Multifunction Interface (CN16), the SyncBus I/O connector (CN11) should not have any attached connections. The SyncBus on the Multifunction Interface is enabled using the SYNC_CTRL register (page 40).

5.6 Serial Peripheral Interface (SPI) Connections

The Multifunction Interface (CN16) of the SPM34CP features a SPI bus with four chip selects. Onboard registers for using the SPI bus are documented on page 43.

For the necessary protocols to establish communication with the SPI device you are attempting to connect, refer to the device's manufacturer documentation.

6 Register Address Space

This section contains board-level control registers that operate at fixed offsets over the Texas Instruments TMS320C6678 EMIF16 interface using the EMIF16 CE0 space. In the physical memory of the TMS320C6678 chip, the EMIF16 CE0 space starts at 0x70000000.

Register Types

There are several different types of registers that are referred to in this section. A description of each type is below.

- Read/Write Registers: The value that is written to this register can also be read back.
- Maskable Registers: This is a 32-bit register that consists of 16-bit data field in the upper word and a 16-bit mask value in the lower word. For each bit in the data field, it is only written to the register if the corresponding bit in the mask field is '1'.
- Sticky Registers: This is a status read register. When a bit in this register has a value of '1', a '1' needs written to that bit to reset the register to '0'. This is typically used for interrupt status registers.
- Read Only: This register can only be read.

NOTE: Writing to Read-Only registers may have unexpected results.

Behavior on a Power Cycle or RESET#

Cycling input power to the SPM34CP or asserting the RESET# input on the Utility Connector (CN5) will result in resetting all registers on the TI C6678's EMIF16 interface to their default state.

6.1 Board Version Registers

Table 26: Register Map: Version Information

Offset	0x03	0x02	0x01	0x00
Base + 0x000	*Reserved*			
Base + 0x004	*Reserved*			
Base + 0x008	SVN_REVISION			
Base + 0x00C	*Reserved*			PDP_REVISION
Base + 00x10	*Reserved*			BRD_VERSION

6.1.1 SVN_REVISION (READ-ONLY)

Contains board revision information. Contact the factory for more information.

6.1.2 PDP_VERSION (READ-ONLY)

Contains board revision information. Contact the factory for more information.

6.1.3 BRD_VERSION (READ-ONLY)

Contains board revision information. Contact the factory for more information.

6.2 General Purpose I/O Control

The registers which control the GPIO connector (CN6) are described in the following sections.

Table 27: Register Map: General Purpose I/O Control

Offset	0x03	0x02	0x01	0x00
Base + 0x100	*Reserved*		GPIO_DIRECTION	
Base + 0x104	*Reserved*			GPIO_PWR_EN

6.2.1 GPIO_DIRECTION (READ/WRITE)

The General Purpose I/O (GPIO) connector (CN6) provides 14 +5V tolerant 3VTTL bit-programmable I/O pins which pass through the board's FPGA to connect directly to the TI DSP pins GP[13:0]. The high or low state of the pins is controlled entirely from the state of the corresponding DSP GPIO pins, as the GPIO port of the DSP is routed to the pins through the FPGA. Thus, the GPIO_DIRECTION register only control over the direction of the pins, and their values.

To configure any I/O pin on the connector as an output, set the FPGA register bit corresponding to the DSP's GPIO pin. To configure as any pin as an input, clear the corresponding bit.

- B[15:14]: *Reserved*
- B[13:0]: Set the pin direction of the General Purpose I/O connector (CN6) pins 14 down to 1 (which correspond to the DSP pins GP[13:0])

Configuring the direction of the FPGA I/O pins must coincide with configuring the direction of the GP[13:0] pins of the DSP, while carefully taking into consideration the order of which each device's pin directions are set. Failing to consider the direction could result in the signals having multiple drivers.

To configure the pin as an input:

1. Configure the direction of the DSP GP pin as an input using the DSP registers.
2. Configure the direction of the FPGA I/O signal as an input by using the GPIO_DIRECTION register.

To configure the pin as an output:

1. Configure the direction of the FPGA I/O signal as an output by using the GPIO_DIRECTION register.
2. Configure the direction of the DSP GP pin as an output using the DSP registers.

An example program is provided on the SPM34CP companion CD which demonstrates configuring the direction of the GPIO pins on the DSP chip as well as the FPGA.

6.2.2 GPIO_PWR_EN (READ/WRITE)

The GPIO_PWR_EN register is used to control the current limited power output pin (+5V_GPIO, pin 16) on the GPIO connector (CN6).

- B[15:1]: *Reserved*
- B[1]: GPIO_PWR_EN: Set to '1' to turn the +5V_GPIO pin ON. Clear to '0' to turn the +5V_GPIO pin OFF.

The +5V_GPIO pin is configured to ON by default.

6.3 LED, Utility, and USER_ID Control

Table 28: Register Map: LED, Utility, and USER_ID Control

Offset	0x03	0x02	0x01	0x00
Base + 0x200	*Reserved*			LED_COLOR
Base + 0x204	*Reserved*			BOOT_MODE
Base + 0x208	*Reserved*			UTIL_PWR_EN
Base + 0x20C	*Reserved*			

6.3.1 LED_COLOR (READ/WRITE)

The SPM34CP has an onboard multi-color red/green/blue LED which can be set by using this register. The Utility Connector (CN5) has corresponding red/green/blue signals which will match the polarity of the bits in this register. The default register setting is red.

To turn on any individual component color of the LED, set the corresponding bit to '1'.

- B[7:3]: *Reserved*
- B[2]: Set to '1' to turn ON the blue component of the LED. Clear to '0' to turn OFF the blue component.
- B[1]: Set to '1' to turn ON the green component of the LED. Clear to '0' to turn OFF the green component.
- B[0]: Set to '1' to turn ON the red component of the LED. Clear to '0' to turn OFF the red component.

The following table lists the color displayed for each value written:

Table 29: Register Map: LED_COLOR Codes

B[2:0]	LED Color
000	Black
111	White
001	Red (default)
011	Yellow
010	Green
110	Cyan
100	Blue
101	Magenta

6.3.2 BOOT_MODE (READ-ONLY)

The BOOT_MODE register indicates the current position of the Boot Selector Switch (SW1). The following table lists the value which the register will display for each position of the switch, along with the corresponding boot mode:

Table 30: Register Map: BOOT_MODE Codes

B[2:0]	Switch Position (SW1)	Boot Mode
000	0	PCIe Boot (requires a host cpuModule)
111	1	Boot to SPI Flash with starting address 0x00100000 (64k)
001	2	Boot to SPI Flash with starting address 0x00400000 (4M)
011	3	Boot to SPI Flash with starting address 0x00800000 (8M)
010	4	Boot to SPI Flash with starting address 0x00C00000 (12M)
110	5	Ethernet Boot
100	6	*Reserved*
101	7	*Reserved*

For more information on the Boot Selection Switch (SW1), see page 26.

For more information on the SPI Flash sectors, see page 34.

6.3.3 UTIL_PWR_EN (READ/WRITE)

The UTIL_PWR_EN register is used to control the current limited power output pin (+5V_UTIL, pin 6) on the Utility Connector (CN5).

- B[15:1]: *Reserved*
- B[1]: UTIL_PWR_EN: Set to '1' to turn the +5V_UTIL pin ON. Clear to '0' to turn the +5V_UTIL pin OFF.

The +5V_UTIL pin is configured to ON by default.

6.4 SyncBus Control

Registers for controlling the SyncBus are described in the sections below. For details on how the SyncBus works, refer to page 36.

Table 31: Register Map: SyncBus Control

Offset	0x03	0x02	0x01	0x00
Base + 0x300	*Reserved*			SYNC_CTRL
Base + 0x304	*Reserved*			SYNC_DI
Base + 0x308	*Reserved*			SYNC_DO
Base + 0x30C	*Reserved*			SYNC_OUT_EN
Base + 0x310	*Reserved*			SYNC_MODE
Base + 0x314	SYNC_TICK_0			
Base + 0x318	SYNC_TICK_1			
Base + 0x31C	SYNC_TICK_2			
Base + 0x320	*Reserved*			
Base + 0x324	*Reserved*			

6.4.1 SYNC_CTRL (READ/WRITE)

- B[7:5]: *Reserved*
- B[2]: When using the SyncBus, the first and last module connected to the SyncBus need to have termination enabled. Set to '1' to enable SyncBus termination. Clear to '0' to disable the termination.
- B[1]: Set to '1' to connect the SyncBus to the Multifunction Interface (CN16). Clear to '0' to connect the SyncBus to the onboard SyncBus I/O header (CN11).
- B[0]: Set to '1' to enable the SyncBus driver. Clear to '0' to disable the driver. When the SyncBus driver is disabled, the transceiver is powered down and SyncBus will not receive or transmit. This bit must be enabled in order to use the SyncBus.

6.4.2 SYNC_DI (READ-ONLY)

When the SyncBus is configured for GPIO mode (with the SYNC_MODE register), the contents of the given SYNC_DI register bit will display the data read on the SyncBus pair which corresponds to that bit.

- B[7:4]: *Reserved*
- B[3]: Data read from SYNC3p/n when the SyncBus is configured for GPIO mode.
- B[2]: Data read from SYNC2p/n when the SyncBus is configured for GPIO mode.
- B[1]: Data read from SYNC1p/n when the SyncBus is configured for GPIO mode.
- B[0]: Data read from SYNC0p/n when the SyncBus is configured for GPIO mode.

6.4.3 SYNC_DO (READ/WRITE)

When the SyncBus is configured for GPIO mode (with the SYNC_MODE register), and the SyncBus pair of interest is enabled to have data driven on it (with the SYNC_OUT_EN register), the contents of the given SYNC_DO register bit will then be driven to the SyncBus pair which corresponds to that bit.

- B[7:4]: *Reserved*
- B[3]: Data be to driven on SYNC3p/n when the SyncBus is configured for GPIO mode and SYNC_OUT_EN is set.
- B[2]: Data be to driven on SYNC2p/n when the SyncBus is configured for GPIO mode and SYNC_OUT_EN is set.
- B[1]: Data be to driven on SYNC1p/n when the SyncBus is configured for GPIO mode and SYNC_OUT_EN is set.
- B[0]: Data be to driven on SYNC0p/n when the SyncBus is configured for GPIO mode and SYNC_OUT_EN is set.

6.4.4 SYNC_OUT_EN (READ/WRITE)

The SYNC_OUT_EN register is used only when the SyncBus pairs are configured as GPIO pin pairs. To permit data to be driven to a SyncBus pair (via the SYNC_DO register), the driver for the given signal pair must be enabled by setting the corresponding bit for that pair to '1'. To disable the driver, clear the bit to '0'.

- B[7:4]: *Reserved*
- B[3]: Set to '1' to enable the driver for SYNC3p/n. Clear to '0' to disable the pair.
- B[2]: Set to '1' to enable the driver for SYNC2p/n. Clear to '0' to disable the pair.
- B[1]: Set to '1' to enable the driver for SYNC1p/n. Clear to '0' to disable the pair.
- B[0]: Set to '1' to enable the driver for SYNC0p/n. Clear to '0' to disable the pair.

6.4.5 SYNC_MODE (READ/WRITE)

The SyncBus differential pairs may be configured to be used as either SyncBus connections or GPIO pin pairs. To set the mode for each signal pair, set the corresponding bit for that to '1' for SyncBus mode. Clear the bit to '0' for GPIO mode.

- B[7:4]: *Reserved*
- B[3]: Set to '1' to configure SYNC3p/n for SyncBus mode. Clear the bit to '0' for GPIO mode.
- B[2]: Set to '1' to configure SYNC2p/n for SyncBus mode. Clear the bit to '0' for GPIO mode.
- B[1]: Set to '1' to configure SYNC1p/n for SyncBus mode. Clear the bit to '0' for GPIO mode.
- B[0]: Set to '1' to configure SYNC0p/n for SyncBus mode. Clear the bit to '0' for GPIO mode.

6.4.6 SYNC_TICK_0, SYNC_TICK_1 , SYNC_TICK_2 (READ/WRITE)

The SPM34CP provides a clock generator on SYNC3p/n which outputs a 10MHz clock.

When the other three other 3 lanes (SYNC0p/n, SYNC1p/n, and SYNC2p/n) are configured as outputs, the SYNC_TICK_0, SYNC_TICK_1, and SYNC_TICK_2 registers may be used to provide a reduced version of the 10MHz clock by dividing it down to the desired frequency.

Each SYNC_TICK_X register is 32 bits wide. The tick frequency for the given lane is set by the following formula:

- B[31:0]: The desired clock rate for the given lane = [10MHz / (n + 1)], where *n* is the value written to the SYNC_TICK_X register

For example:

- If you write a 1 to the register, the given SyncBus lane will output a 5MHz clock which is synchronized to the 10MHz clock on SYNC3p/n.
- If you set the register to 99, the SyncBus lane will output a 100kHz clock which is synchronized to the 10MHz clock on SYNC3p/n
- If you set the register to 2^32-1, the SyncBus lane will provide a tick every 430s, synchronized to the 10MHz clock on the SYNC3p/n

6.5 Ethernet Status

The Ethernet control registers in this section pertain to the behavior of the Ethernet switch subsystem, connections CN20 & CN30.

Table 32: Register Map: Ethernet Control

Offset	0x03	0x02	0x01	0x00
Base + 0x400	*Reserved*			ETH_LED
Base + 0x404	*Reserved*			

6.5.1 ETH_LED (READ-ONLY)

- B[7:3]: *Reserved*
- B[2]: Toggles to indicates link activity on Ethernet connector CN20
- B[1]: *Reserved*
- B[0]: Toggles to indicates link activity on Ethernet connector CN30

6.6 Serial Port Transceiver Control

Table 33: Register Map: Serial Port Transceiver Control

Offset	0x03	0x02	0x01	0x00
Base + 0x500	*Reserved*			SER_PORT_CTRL

6.6.1 SER_PORT_CTRL (READ/WRITE)

- B[7]: Set to '1' to enable termination on the RXD+/- pair when in RS-422 mode and the D+/- pair when in RS-485. Clear to '0' to disable termination.
- B[6]: This bit enables/disables drivers in the serial port transceiver for connector CN7, but the exact function is dependent on the setting of B[3:1]. See the table for B[3:1] for the exact function.
- B[5]: *Reserved*
- B[4]: Set to '1' to limit the slew rate of the serial port transceiver drivers. Set to '0' to use the standard slew rate.
- B[3:1]: Sets the mode for connector CN7's serial port transceiver

Table 34: Register Map: SER_PORT_CTRL Mode Selection

Serial Port (CN7) Mode	B[3:1] Value	B[6] Function
RS-232	0x1	*Don't Care*
RS-422	0x3	Set to '1' = Transmitter Enable, Receiver Disable Clear to '0' = Transmitter Disable, Receiver Enable
RS-485	0x2	Set to '1' = Transmitter Enable Clear to '0' = Transmitter Disable

- B[0]: Set to '1' to enable the serial port transceiver for connector CN7

6.7 SPI Bus Control

The SPI bus controller registers are used for programming the four SPI device connections on the Multifunction Interface (CN16). More information on the SPI bus connections can be found on page 36.

Table 35: Register Map: SPI Bus Control

Offset	0x03	0x02	0x01	0x00
Base + 0x580	SPI_WR_DATA *(upper 32-bits)*			
Base + 0x584	SPI_WR_DATA *(lower 32-bits)*			
Base + 0x588	*Reserved*			
Base + 0x58C	*Reserved*			
Base + 0x590	SPI_RD_DATA			
Base + 0x594	*Reserved*			
Base + 0x598	*Reserved*			
Base + 0x59C	*Reserved*			
Base + 0x5A0	*Reserved*			SPI_START
Base + 0x5A4	*Reserved*			SPI_BUSY
Base + 0x5A8	*Reserved*			
Base + 0x5AC	*Reserved*			
Base + 0x5B0	*Reserved*			SPI_CS_LENGTH
Base + 0x5B4	*Reserved*			SPI_PHASE
Base + 0x5B8	*Reserved*			SPI_POLARITY
Base + 0x5BC	*Reserved*			SPI_BIT_SLIP

6.7.1 SPI_WR_DATA (READ/WRITE)

- B[63:0]: Data to be written during a SPI transaction

6.7.2 SPI_RD_DATA (READ-ONLY)

- B[31:0]: Data to be read during a SPI transaction

6.7.3 SPI_START (READ/WRITE)

To begin a transaction with one of the SPI devices on the Multifunction Interface (CN16), set the value to '1' for the register which corresponds to that SPI device. Clear the given bit to '0' when the device is unused.

- B[7:3]: *Reserved*
- B[3]: Set to '1' to select the device connected to SPI_CS3#. When the device is unused, the bit should be cleared to '0'.
- B[2]: Set to '1' to select the device connected to SPI_CS3#. When the device is unused, the bit should be cleared to '0'.
- B[1]: Set to '1' to select the device connected to SPI_CS3#. When the device is unused, the bit should be cleared to '0'.
- B[0]: Set to '1' to select the device connected to SPI_CS3#. When the device is unused, the bit should be cleared to '0'.

6.7.4 SPI_BUSY (READ-ONLY)

Poll the SPI_BUSY register to check the status of the transaction being processed.

- B[7:1]: *Reserved*
- B[0]: Returns '1' if the current transaction is incomplete. Returns '0' after the transaction has completed.

6.7.5 SPI_CS_LENGTH (READ/WRITE)

This register specifies the length of the transaction in bytes.

- B[7:0]:
  - 0x00: Indicates that 1 byte of data is to be transmitted or received.
  - 0x01: Indicates that 2 bytes of data are to be transmitted or received.
  - 0x02: Indicates that 3 bytes of data are to be transmitted or received.
  - 0x03: Indicates that 4 bytes of data are to be transmitted or received.
  - 0x04: Indicates that 5 bytes of data are to be transmitted or received.
  - 0x05: Indicates that 6 bytes of data are to be transmitted or received.
  - 0x06: Indicates that 7 bytes of data are to be transmitted or received.
  - 0x07: Indicates that 8 bytes of data are to be transmitted or received.

6.7.6 SPI_PHASE (READ/WRITE)

This register sets the SPI phase.

- B[7:1]: *Reserved*
- B[0]: Set to '1' to shift in at PACE_END, that is at falling edge. Clear to '0' to shift in at PACE_HALF, that is at rising edge.

When the SPI_PHASE register is configured for PACE_HALF, the SPI_BIT_SLIP register should also be configured.

6.7.7 SPI_POLARITY (READ/WRITE)

This register sets the SPI polarity.

- B[7:1]: *Reserved*
- B[0]: Set to '1' for active-high polarity. Clear to '0' for active-low polarity.

6.7.8 SPI_BIT_SLIP (READ/WRITE)

This register sets the SPI bit slip, and should be configured if the SPI_PHASE register is configured for PACE_HALF.

- B[7:1]: *Reserved*
- B[0]:
    - If '0', the first bit is shifted in on the first rising edge
    - If '1', the first bit is shifted in on the second rising edge

7 Troubleshooting

If you are having problems with your system, please try the following initial steps:

- **Simplify the System** – Remove modules one at a time from your system to see if there is a specific module that is causing a problem. Perform you troubleshooting with the least number of modules in the system possible.

- **Swap Components** – Try replacing parts in the system one at a time with similar parts to determine if a part is faulty or if a type of part is configured incorrectly.

If problems persist, or you have questions about configuring this product, contact RTD Embedded Technologies via the following methods:

Phone: +1-814-234-8087
E-Mail: techsupport@rtd.com

Be sure to check the RTD web site (http://www.rtd.com) frequently for product updates, including newer versions of the board manual and application software.

8 Additional Information

8.1 PC/104 Specifications

A copy of the latest PC/104 specifications can be found on the webpage for the PC/104 Embedded Consortium:

www.pc104.org

8.2 PCI and PCI Express Specification

A copy of the latest PCI and PCI Express specifications can be found on the webpage for the PCI Special Interest Group:

www.pcisig.com

8.3 Serial RapidIO® Resources

A copy of the latest RapidIO specification can be found on the webpage for the RapidIO Trade Association:

www.rapidio.org

TI's KeyStone Architecture Serial RapidIO (SRIO) User Guide (Literature Number SPRUGW1B) is a thorough guide describing the general operation of the RapidIO system on the TMS320C6678 and how to use it to connect the outside world. The document can be found on TI's website.

www.ti.com

8.4 TI Resources

The TMS320C6678 Digital Signal Processor on the SPM34CP is a very complex device. A full description of its internal functions and registers is beyond the scope of this document. Full documentation is supplied by Texas Instruments. TI also supplies application notes to demonstrate many of the functions of this DSP. For more information, refer TI's website.

www.ti.com

TI provides a set of user forums through the TI E2E Community which include forums for developers working with the TMS320C6678, Code Composer Studio, Linux, and much more. For more information, refer to the TI E2E Community website:

e2e.ti.com

9 Limited Warranty

RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD Embedded Technologies, Inc. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, RTD Embedded Technologies will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to RTD Embedded Technologies. All replaced parts and products become the property of RTD Embedded Technologies. Before returning any product for repair, customers are required to contact the factory for a Return Material Authorization (RMA) number.

This limited warranty does not extend to any products which have been damaged as a result of accident, misuse, abuse (such as: use of incorrect input voltages, improper or insufficient ventilation, failure to follow the operating instructions that are provided by RTD Embedded Technologies, “acts of God” or other contingencies beyond the control of RTD Embedded Technologies), or as a result of service or modification by anyone other than RTD Embedded Technologies. Except as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranties of merchantability and fitness for a particular purpose, and RTD Embedded Technologies expressly disclaims all warranties not stated herein. All implied warranties, including implied warranties for merchantability and fitness for a particular purpose, are limited to the duration of this warranty. In the event the product is not free from defects as warranted above, the purchaser's sole remedy shall be repair or replacement as provided above. Under no circumstances will RTD Embedded Technologies be liable to the purchaser or any user for any damages, including any incidental or consequential damages, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

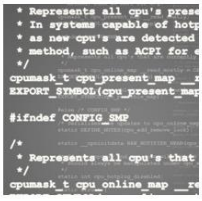
Some states do not allow the exclusion or limitation of incidental or consequential damages for consumer products, and some states do not allow limitations on how long an implied warranty lasts, so the above limitations or exclusions may not apply to you.

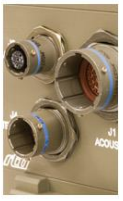
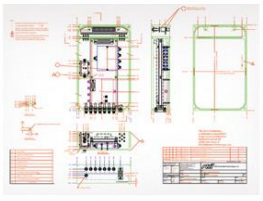
This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

RTD Embedded Technologies, Inc.
103 Innovation Boulevard
State College, PA 16803 USA
Telephone: 814-234-8087
Fax: 814-234-5218

www.rtd.com

sales@rtd.com
techsupport@rtd.com



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