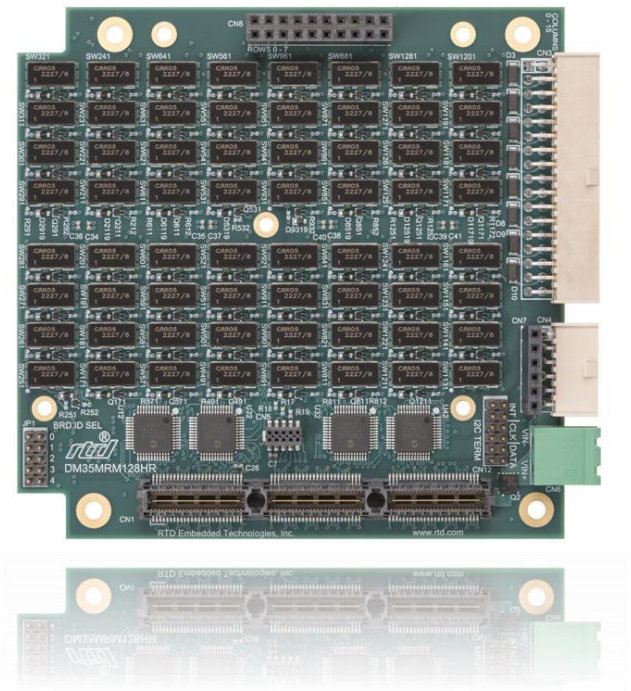
DM35MRM128HR

8x16 Switch Matrix

User's Manual

BDM-610020160 Rev. A



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PC/104

DESIGNED AND MADE IN THE UNITED STATES

AS9100 - ISO 9001 CERTIFIED

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Rev A	Initial Release

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1 Introduction

1.1 Product Overview

The DM35MRM128HR is a stackable switch matrix module. This module consists of an 8x16 array of single pole (form A) rhodium contact reed relays. Each relay can be individually closed to connect a single column to a single row, and a combination of relay closures can form any desired network of connections. This allows software to freely connect and disconnect any one I/O pin in the matrix to any number of other pins. By stacking or cabling together additional DM35MRM128HR modules, the 8x16 matrix can expand up to 8x512.

The switch matrix module features the NXP PCA9616 buffer to provide differential I2C communication. This buffer increases the allowable distance of use and reduces signal noise over the standard I2C protocol. These two factors make the DM35MRM128HR ideal for remotely controlled solutions.

To reduce hardware and software development time, the DM35MRM128HR can be combined with RTD's CM35I2C03HR. This provides the user with Operating System drivers and example programs that immediately demonstrate the functionality of the module

1.2 Board Features

- PC/104 form factor
- PCIe/104 stackable bus structure
  - PCIe universal expansion bus (Type 1 or Type 2)
- Switch Matrix:
  - Designed with Form A contacts
  - 128 Crosspoint Switch Matrix expandable to 4096
  - 16 columns expandable up to 512
  - 8 rows
- Differential I2C communication using NXP PCA9616
  - Support 1Mhz over 3 meters.
  - Onboard jumper termination
- External power connector for cabled solution
  - 12V input
  - Reverse Polarity Protection
  - Input Voltage Transient Protection
- Relay I/O
  - Max Voltage: 100 V_{DC}, 100 V_{AC}
  - Max Current: 0.5A Per Channel (10 W Max)
  - Expected life:
    - Mechanical: $5x10^8$ cycles
    - Electrical
      - 10V, 100mA: 10^7 cycles
      - 20V, 500mA: $5x10^6$ cycles
      - 100V, 10mA: $5x10^5$ cycles
- Available in stackable, rugged enclosures
- Requires +12 VDC for operation

1.3 Ordering Information

The DM35MRM128HR is available with the following options:

Table 1: Ordering Options

Part Number	Description
DM35MRM128HR	PCIe/104 128 Crosspoint Switch Matrix Module

The Intelligent Data Acquisition Node (IDAN®) building block can be used in just about any combination with other IDAN building blocks to create a simple but rugged 104™ stack. This module can also be incorporated in a custom-

built RTD HiDAN® or HiDAN*plus*® High Reliability Intelligent Data Acquisition Node. Contact RTD sales for more information on our high reliability systems.

1.4 Contact Information

1.4.1 Sales Support

For sales inquiries, you can contact RTD Embedded Technologies sales via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: sales@rtd.com

1.4.2 Technical Support

If you are having problems with your system, please try the steps in the Troubleshooting section of this manual on page 25.

For help with this product, or any other product made by RTD, you can contact RTD Embedded Technologies technical support via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: techsupport@rtd.com

2 Specifications

2.1 Operating Conditions

Table 2: Operating Conditions

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{cc5}	5V Supply Voltage		n/a	n/a	V
V_{cc3}	3.3V Supply Voltage		n/a	n/a	V
V_{cc12}	12V Supply Voltage		11.4	12.6	V
V_{cc-12}	-12V Supply Voltage		n/a	n/a	V
T_a	Operating Temperature		-40	+85	C
T_s	Storage Temperature		-55	+125	C
RH	Relative Humidity	Non-Condensing	0	90%	%
MTBF	Mean Time Before Failure	Telcordia Issue 2 30°C, Ground benign, controlled		TBD	Hours

2.2 Electrical Characteristics

Table 3: Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Switch Specification						
	Switch Type	Rhodium Reed				
	Switching Voltage	Channel-to-Channel			100	V_{AC}
	Switch Power				10	W
	Switch Current				0.5	A
	Carry Current					
	Closed Switch Path			0.5		Ω
	Open Switch Path					Ω
	Bandwidth	-3 dB, 50 Ω termination				dB
	Channel-to-channel crosstalk	10 kHz				dB
		100 kHz				dB
		1 Mhz				dB

3 Board Connection

3.1 Board Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your board in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the board at the edges, and do not touch the components or connectors. Handle the board in an antistatic environment and use a grounded workbench for testing and handling of your hardware.

3.2 Physical Characteristics

STEP model is available upon request; contact RTD Tech Support for more information.

- Weight: Approximately 0.25 lbs. (0.11 Kg)
- Dimensions: 4.10 in. L x 3.775 in. W (104.14 mm L x 95.89 mm W)

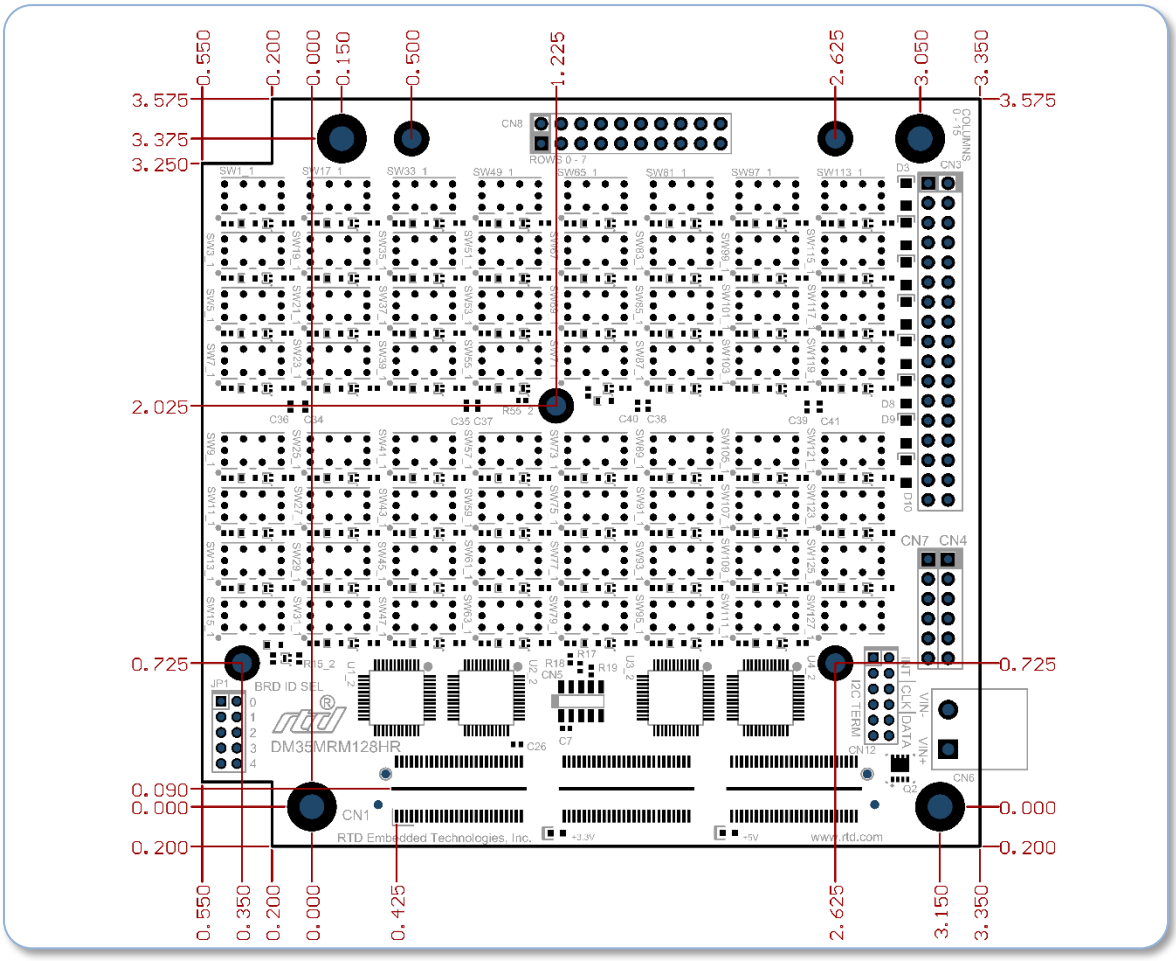


Figure 1: Board Dimensions

3.3 Connectors and Jumpers

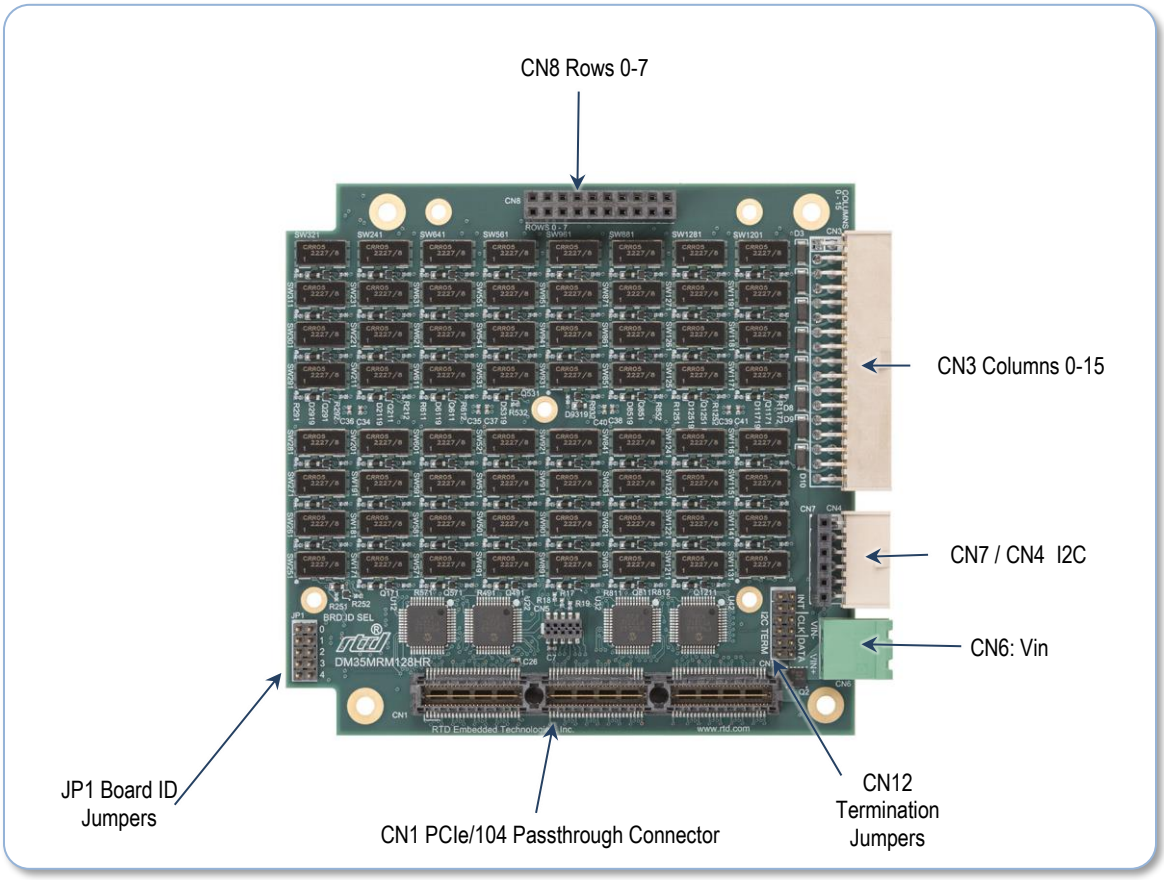


Figure 2: Board Connections

3.3.1 External I/O Connectors

CN8: Rows Connector

CN8 is a 20 pin 0.1" stack through connector. Pin 1 is indicated by a square pad on the bottom of the board.

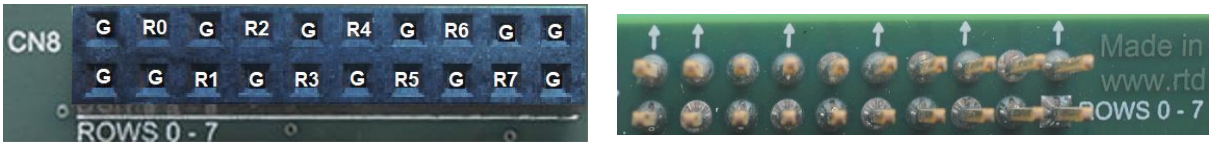


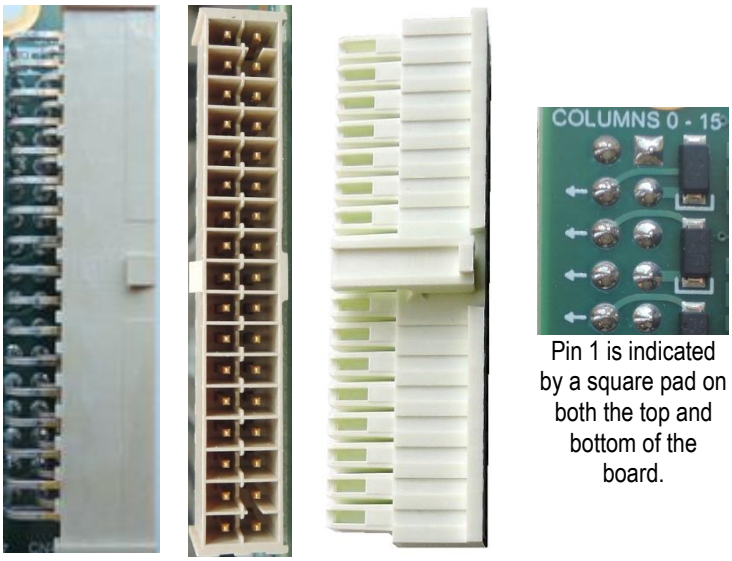
Figure 3 CN8 Rows Connector

2	4	6	8	10	12	14	16	18	20
GND	ROW 0	GND	ROW 2	GND	ROW 4	GND	ROW 6	GND	GND
GND	GND	ROW 1	GND	ROW 3	GND	ROW 5	GND	ROW 7	GND
1	3	5	7	9	11	13	15	17	19

Table 4: CN8 Rows Connector Pin Assignments

CN3: Columns Connector

CN3 is a 34 pin 0.1” right angle connector. An example of its mating connector is the Samtec IPD1-17-D-K (shown on below).



Pin 1 is indicated by a square pad on both the top and bottom of the board.

Figure 4: CN3 Columns Connector

2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
COL 0	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7	COL 8	COL 9	COL 10	COL 11	COL 12	COL 13	COL 14	COL 15	GND
1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33

Table 5: CN3 Columns Connector Pin Assignments

CN4: Cabled I2C Connector

CN4 is a 0.1” 6-pin right angle cabled I2C connector. An example of its’ mating connector is the Samtec IPD1-06-S-K (shown on right).

CN4: Cabled I2C Connector

CN4 is a 0.1” 6-pin right angle cabled I2C connector. An example of its’ mating connector is the Samtec IPD1-06-S-K. Pin 1 is indicated by a square pad on both the top and bottom of the board.

Figure 5: CN4 Cabled I2C Connector

1	2	3	4	5	6
I2C_INT_P	I2C_INT_N	I2C_CLK_N	I2C_CLK_P	I2C_DATA_P	I2C_DATA_N

Table 6 CN4 Cabled I2C Connector Pin Assignments

CN7: Stack through I2C Connector

CN7 is a 6-pin vertical 0.1" I2C connector. An example of its' mating connector is the Samtec HTSW-106-05-F-S header. Pin 1 is indicated by a square pad on both the top and bottom of the board.

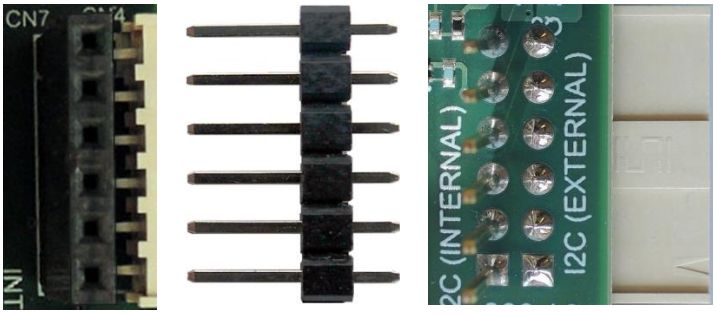


Figure 6: CN7 Stack through I2C Connector

CN6: Vin power input

CN6 is a two-pin power input connector. An example of a mating connector is the Phoenix Contact 1779987. Pin 1 is indicated by a square pad on the bottom of the board.

Figure 7: CN6 Vin Power Connector

VIN-	2	1	VIN+

Figure 8: CN6 Vin Power Connector Pin Assignments

3.3.2 BUS CONNECTORS

CN1(Top) & CN2(Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 26)

The DM35MRM128HR is a "Universal" board and can connect to either a Type 1 or Type 2 PCIe/104 connector.

CN16: PCI Connector

The PCI connector is the connection to PCI peripheral modules. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 26)

3.3.3 JUMPERS

JP1: Board ID

JP1 is used to configure the boards I²C base address. The JP1 jumpers are used to set the 5 most-significant bits of the address. The lower 3 bits are used for the follow:

- Bit 1&2: Onboard controller address
- Bit 0: Read/Write

The table on the following pages shows the possible I²C base address settings for the DM35MRM128HR. All base addresses are in hexadecimal. An 'X' indicates a closed jumper, while an empty cell indicates an open jumper.

I2C base address (Hexadecimal)	Jumpers				
	4	3	2	1	0
00					
08					X
10				X	
18				X	X
20			X		
28			X		X
30			X	X	
38			X	X	X
40		X			
48		X			X
50		X		X	
58		X		X	X
60		X	X		
68		X	X		X
70		X	X	X	
78		X	X	X	X
80	X				
88	X				X
90	X			X	
98	X			X	X
A0	X		X		
A8	X		X		X
B0	X		X	X	
B8	X		X	X	X
C0	X	X			
C8	X	X			X
D0	X	X		X	
D8	X	X		X	X
E0	X	X	X		
E8	X	X	X		X
F0	X	X	X	X	
F8	X	X	X	X	X

Table 7: I2C base address

3.4 Steps for Installing

1. Always work at an ESD protected workstation and wear a grounded wrist-strap.
2. Turn off power to the PC/104 system or stack.
3. Select and install stand-offs to properly position the module on the stack.
4. Remove the module from its anti-static bag.
5. Check that pins of the bus connector are properly positioned.
6. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
7. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
8. Gently and evenly press the module onto the PC/104 stack.
9. If any boards are to be stacked above this module, install them.
10. Attach any necessary cables to the PC/104 stack.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all the hardware is working properly.

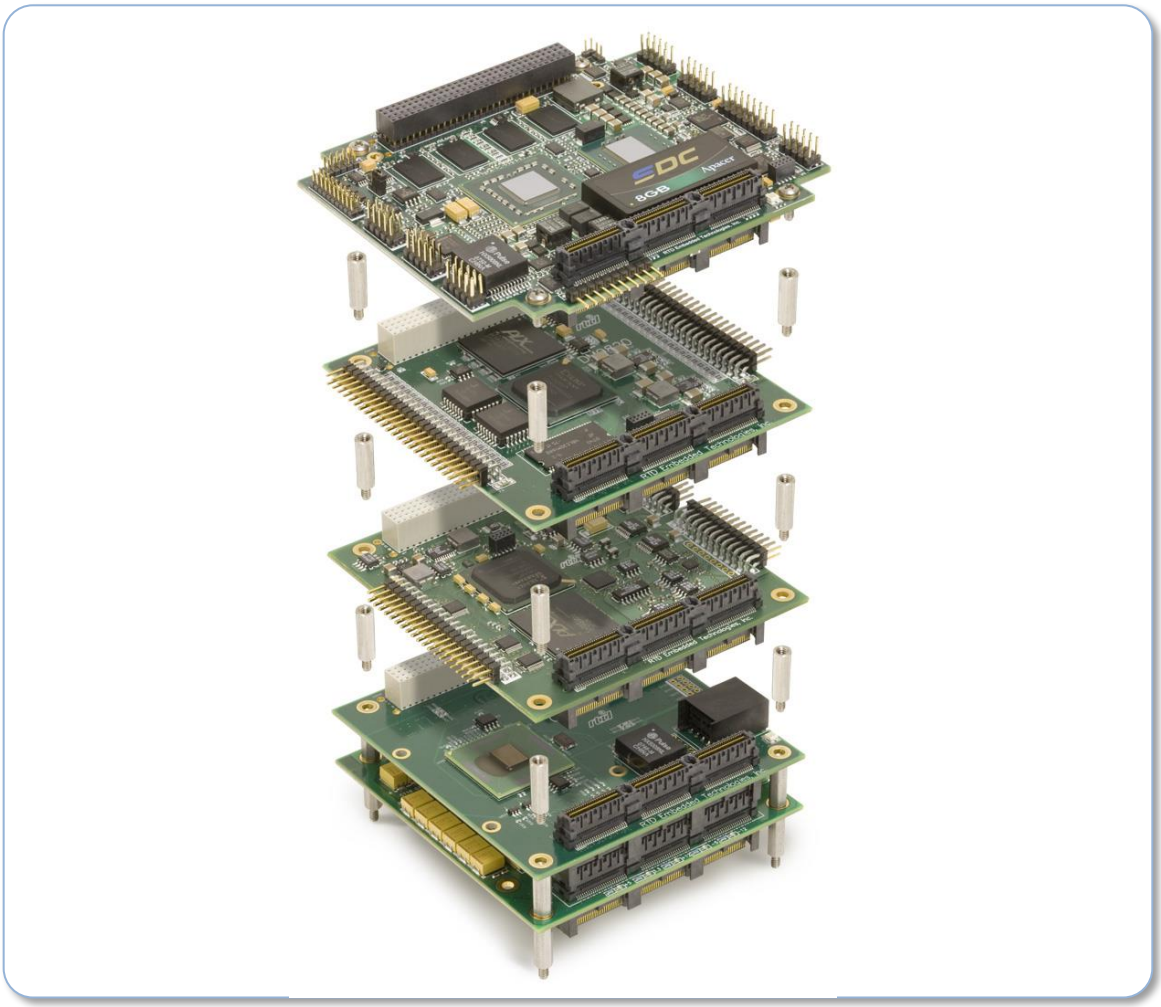


Figure 9: Example 104™ Stack

4 Functional Description

4.1 Block Diagram

The Figure below shows the functional block diagram of the DM35MRM128HR. The various parts of the block diagram are discussed in the following sections.

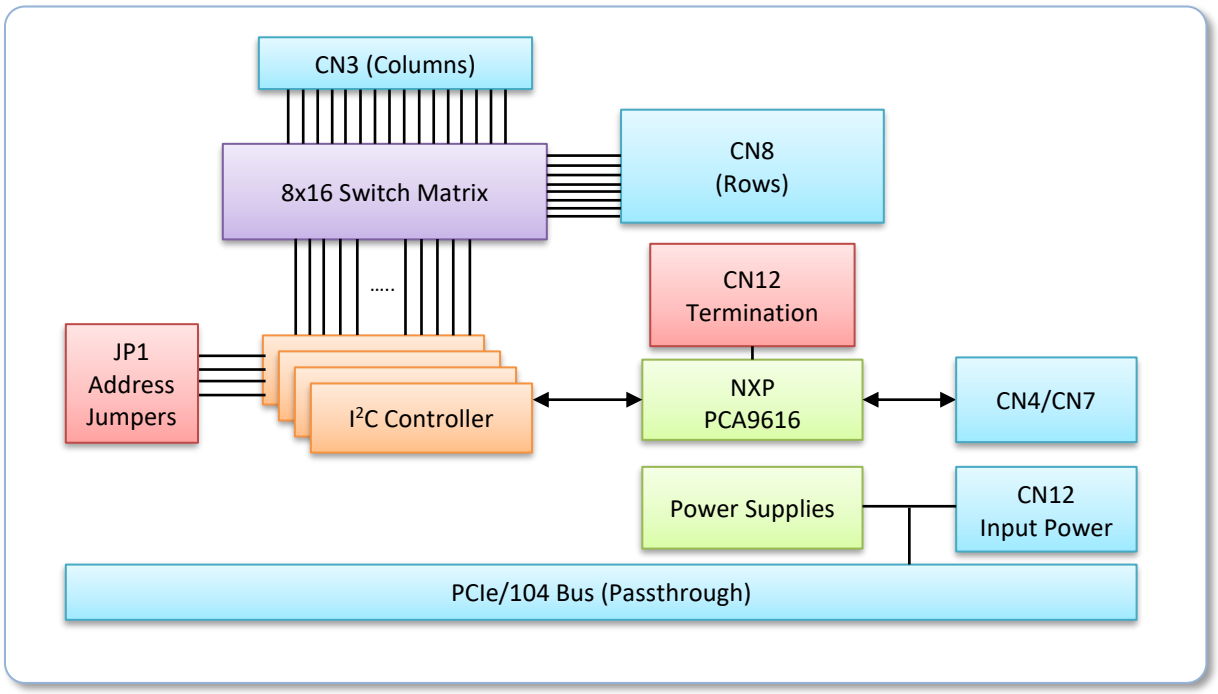


Figure 10: DM35MRM128HR Block Diagram

4.2 I²C Communication Bus

The DM35MRM128HR controls the switch matrix through an I²C slave interface. This module utilizes a differential I²C buffer to provide a long distance and increase noise immunity for remote cable solution. Typical I²C communication is limited to under 1m distance, however with the use the differential buffer we can achieve up to 3m cabling at 1Mhz clock rates. At lower clock speeds this distance can extend much farther.

To communicate with the DM35MRM128HR the user must have I²C host controller. RTD's CM35I2C03HR provides host card solution for the DM35MRM128HR. The CM35I2C03HR is a PCIe interface that provides 3 independent differential I²C bus. The module allows in-stack solution or remote cabling to the DM35MRM128HR. RTD provides example programs for DM35MRM128HR using the CM35I2C03HR host controller.

4.2.1 Host Controller Information

In this section RTD provides information about the NXP PCA9616 buffer that is used on the DM35MRM128HR to provide the differential I²C bus. If you do not use the CM35I2C03HR as a host I²C host, the information below can be used to develop a differential I²C interface for your host module.

NXP PCA9616 Buffer

Figure 11 below is an example circuit for the NXP PCA9616. The single ended I²C (pins 2, 4, 7) will need to be connected to the I²C host controller, as the DM35MRM128HR is a salve device. The differential I²C (pins 10-15) will need to be wired to CN4 see section CN4: Cabled I2C Connector on page 12. The DM35MRM128HR has $V_{DD(B)}$ set to 5V, the host side needs to be the same.

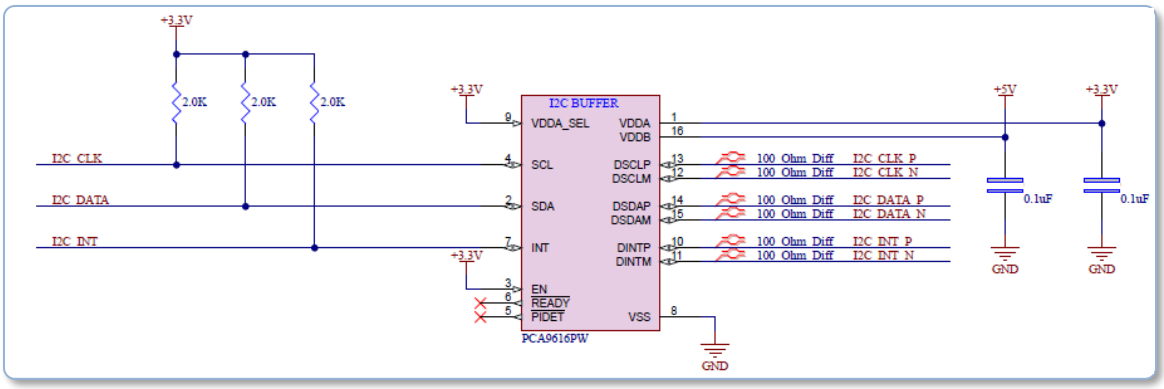


Figure 11: NXP PCA9616 Example Circuit

Termination Circuit

Typical single-ended I²C is not suited for long distance due to ringing and reflections. The use of termination and differential signaling minimizes this issue. The DM35MRM128HR provides 5V to the $V_{DD(B)}$ of the PCA9616, the termination pull resistors should be pulled to 5V, as shown in Figure 12. When designing a host controller, you must provide termination, as it will end point.

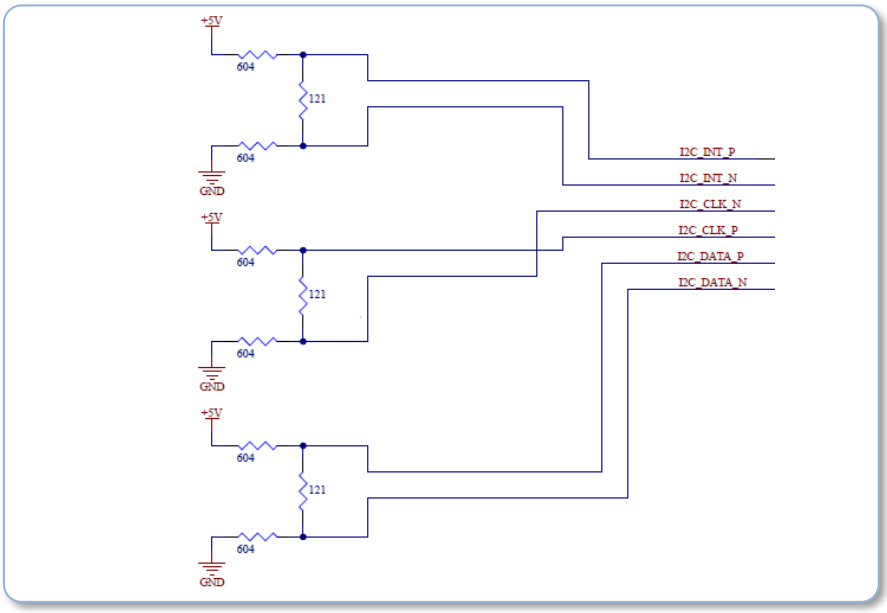


Figure 12: PCA9616 Termination

4.2.2 Differential Cabling

The differential I²C interface is designed for 100Ω impedance transmission lines. Using the termination circuit shown above, RTD suggest using CAT5, CAT6, or CAT7 data cable for cabling between host and slave. CAT5, CAT6 and CAT7 provide 4 twisted pairs, the 4 pairs can be used for 3 signals (INT, CLK, DATA) and power.

4.3 Switch Matrix

The DM35MRM128HR is a high-density matrix module consisting of 8 rows by 16 columns of type A reed relays. This configuration allows for 128 crosspoints. This allows for users to programmatically switch wiring configuration as needed, this makes for a perfect tool for DUT (device under test) testing.

4.3.1 CROSSPOINT MATRIX

Crosspoint switch matrix is made up of vertical and horizontal lines, where they intersect it is called a crosspoint. A relay is located at every crosspoint, as shown below in Figure 13, allowing the row and column to be connected. By the natural of the design there is no limit to the number of connections a particular row or column has, however as more connections are made simultaneously, this increases the load on the signal source.

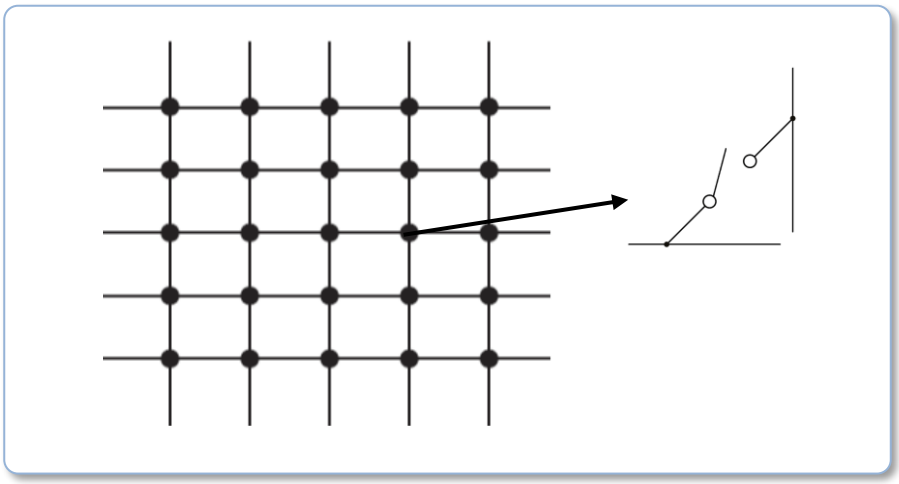


Figure 13: Example 5x5 Matrix Crosspoint

Matrices are defined by rows and columns, rows being the horizontal lines and columns being the vertical lines. Using the 5x5 matrix seen in Figure 13, you can close the crosspoint relay at any row and column connection. With this matrix, you can make five separate connections from the test instruments and the DUT. Making multiple simultaneous connections on either axis is also possible, this is what makes crosspoint matrix extremely flexible.

DM35MRM128HR Configuration

DM35MRM128HR module uses 4 independent I^2C controllers to configure all 128 relays. Each controller used to configure 2 rows, example controller 0 configures row 0 and 1. Each controller has a unique address. This address is configured by the board ID jumpers found in section 3.3.3

5 I²C Interface

5.1 Read Command Set

The figure below provides a summary of the DM35MRM128HR I²C Read Command Set.

Table 8: I²C Read Command Set

Read Address	Name	Register Description
0x00	Write Commands	Count of how many valid write registers are in the module.
0x01	Read Commands	Count of how many valid read registers are in the module.
0x02	Unique Id	An unique number that identifies the register set that is provide by the module. This number will be common among all modules that share the exact register set.
0x03-0x09	Module Name	Module name in ASCII.
0x0A	Flag_Status	Status register See Flag_Status register table for more infomation
0x0B	*Reserved*	*Reserved*
0x0C-0x0D	Bank 0 Status	State of relay enable signals of bank 0. Each bit corresponds to the match column. (e.g. bit 0 controls column 0) Lower Byte corresponds to the columns 0-7 Upper Byte corresponds to the columns 8-15
0x0E-0x0F	Bank 1 Status	State of relay enable signals of bank 1. Each bit corresponds to the match column. (e.g. bit 0 controls column 0) Lower Byte corresponds to the columns 0-7 Upper Byte corresponds to the columns 8-15
0x10	Configuration	Readback of the configuration register. See the configuration register for more information.
0x11-0x30	*Reserved*	*Reserved*
0x31-0x32	Bank 0 Shadow Status	Readback of the shadow register for Bank 0. Each bit corresponds to the match column. (e.g. bit 0 controls column 0) Lower Byte corresponds to the columns 0-7 Upper Byte corresponds to the columns 8-15
0x33-0x34	Bank 1 Shadow Status	Readback of the shadow register for Bank 1 Each bit corresponds to the match column. (e.g. bit 0 controls column 0) Lower Byte corresponds to the columns 0-7 Upper Byte corresponds to the columns 8-15
0x35	Configuration Shadow	Readback of the shadow configuration register. See the configuration register for more information.
0x36-x59	*Reserved*	*Reserved*
0x60-0x63	Build Number	Firmware build number.

5.1.1 Write Commands Register (0x00 Read)

This register contains how many valid write registers are in the module. The DM35MRM128HR has separate read and write pointers. The write pointer starts at 0x00, the last valid write register is value of this register minus one.

Bits	Description
7:0	Number of valid write registers in hex.

5.1.2 READ COMMANDS REGISTER (0X01 READ)

This register contains how many valid read registers are in the module. The DM35MRM128HR has separate read and write pointers. The read pointer starts at 0x00, the last valid read register is value of this register minus one.

Bits	Description
7:0	Number of valid read registers in hex.

5.1.3 UNIQUE ID REGISTER (0X02 READ)

This register contains the modules unique id number. This number will be common among all modules that share the exact register set.

Bits	Description
7:0	Unique number that identifies the register set that is provide by the module in hex.

5.1.4 MODULE NAME REGISTER (0X03-0X09 READ)

The following set of registers contains the modules name. Each of the follow byte is ASCII character that used to identify the module name.

Address	Bits	Description
0x03	7:0	First character in the module name.
0x04	7:0	Second character in the module name.
0x05	7:0	Third character in the module name.
0x06	7:0	Fourth character in the module name.
0x07	7:0	Fifth character in the module name.
0x08	7:0	Sixth character in the module name.
0x09	7:0	Seventh character in the module name.

5.1.5 FLAG_STATUS REGISTER (0X0A READ)

This register contains I^2C controller status flag. The table below provide a description for each bit in the register.

Name	Bits	Description
RSVD	0	*Reserved*
GEN_CALL	1	This flag is set to show if a general call was issued to the I^2C bus. This flag is cleared at a stop condition. 1 – Valid general call was issued 0 – Invalid or no general call was issued
BANK0_ERROR	2	When configured in blocking mode, if more than two relays are enabled this will be set high. 1 – A blocking error occurred on bank 0 0 – No blocking error bank 0
BANK1_ERROR	3	When configured in blocking mode, if more than two relays are enabled this will be set high. 1 – A blocking error occurred on bank 1 0 – No blocking error bank 1
RSVD	4	*Reserved*
GEN_CALL_MATCH	5	This flag is set to show if a general call had a matching unique id to this I^2C controller. 1 – Unique ID matched general call 0 – Unique ID did not match gnernal call
RSVD	7:6	*Reserved*

5.1.6 RESVERED (0X0B)

This register is reserved.

Bits	Description
7:0	*Reserved*

5.1.7 BANK 0 STATUS REGISTER (0X0C-0X0D READ)

This register contains the current state of the bank 0 enable signals. Each bit corresponds to the match column. (e.g. bit 0 controls column 0). It is not required to read both bytes.

Address	Bits	Description
0x0C	7:0	Lower Byte corresponds to the columns 0-7
0x0D	7:0	Upper Byte corresponds to the columns 8-15

5.1.8 BANK 1 STATUS REGISTER (0X0E-0X0F READ)

This register contains the current state of the bank 1 enable signals. Each bit corresponds to the match column. (e.g. bit 0 controls column 0). It is not required to read both bytes.

Address	Bits	Description
0x0E	7:0	Lower Byte corresponds to the columns 0-7
0x0F	7:0	Upper Byte corresponds to the columns 8-15

5.1.9 CONFIGURATION READBACK REGISTER (0X10 READ)

This register contains Configuration Readback Register. The table below provide a description for each bit in the register.

Name	Bits	Description
AUTO_WRITE	0	Status of the AUTO_WRITE function. When AUTO_WRITE is enabled writes into the shadow registers are propagated when a stop condition occurs. 1 – Auto write is enabled 0 – Auto write is disabled
BUS TIMEOUT FLAG	1	Flag used to indicate that an timeout occur on the I^2C Bus. Cleared by writing to configuration register. 1 – Timeout event has occurred 0 – No timeout event has occurred.
BLOCKING MODE	2	Status of BLOCKING_MODE function. BLOCKING_MODE function is hardware implantation to prevent more then 2 connection on a Bank at a time. 1 – Blocking mode is enabled 0 – Blocking mode is disabled
AUTO WRITE READBACK	3	Status of the AUTO_WRITE_READBACK function. When AUTO_WRITE_READBACK is enabled writes into the shadow readback register are updated immediately. 1 – Auto write readback is enabled 0 – Auto write readback is disabled
RSVD	7:4	*Reserved*

5.1.10 RESVERED (0X11-0X30)

These registers are reserved.

Bits	Description
7:0	*Reserved*

5.1.11 BANK 0 SHADOW STATUS REGISTER (0X31-0X32 READ)

This register contains the readback of the bank 0 shadow register. Each bit corresponds to the match column. (e.g. bit 0 controls column 0). It is not required to read both bytes.

Address	Bits	Description
0x0C	7:0	Lower Byte corresponds to the columns 0-7
0x0D	7:0	Upper Byte corresponds to the columns 8-15

5.1.12 BANK 1 SHADOW STATUS REGISTER (0X33-0X34 READ)

This register contains the readback of the bank 1 shadow register. Each bit corresponds to the match column. (e.g. bit 0 controls column 0). It is not required to read both bytes.

Address	Bits	Description
0x0E	7:0	Lower Byte corresponds to the columns 0-7
0x0F	7:0	Upper Byte corresponds to the columns 8-15

5.1.13 CONFIGURATION SHADOW READBACK REGISTER (0X35 READ)

This register contains Configuration Shadow Readback Register. The table below provide a description for each bit in the register.

Name	Bits	Description
AUTO_WRITE	0	Status of the AUTO_WRITE function. When AUTO_WRITE is enabled writes into the shadow registers are propagated when a stop condition occurs. 1 – Auto write is enabled 0 – Auto write is disabled
BUS TIMEOUT FLAG	1	Flag used to indicate that an timeout occur on the I²C Bus. Cleared by writing to configuration register. 1 – Timeout event has occurred 0 – No timeout event has occurred.
BLOCKING MODE	2	Status of BLOCKING_MODE function. BLOCKING_MODE function is hardware implantation to prevent more then 2 connection on a Bank at a time. 1 – Blocking mode is enabled 0 – Blocking mode is disabled
AUTO WRITE READBACK	3	Status of the AUTO_WRITE_READBACK function. When AUTO_WRITE_READBACK is enabled writes into the shadow readback register are updated immediately. 1 – Auto write readback is enabled 0 – Auto write readback is disabled
RSVD	7:4	*Reserved*

5.1.14 RESVERED (0X36-0X59)

These registers are reserved.

Bits	Description
7:0	*Reserved*

5.1.15 BUILD NUMBER REGISTER (0X60-0X63 READ)

The following set of registers contains a unique 32-bit firmware build number. This unique number can help identify what firmware version is running on the module.

Address	Bits	Description
0x60	7:0	Bits 7:0 of the build number
0x61	7:0	Bits 15:8 of the build number
0x62	7:0	Bits 23:16 of the build number
0x63	7:0	Bits 31:24 of the build number

5.2 Write Command Set

The figure below provides a summary of the DM35MRM128HR I²C Write Command Set.

Table 9: I²C Write Command Set

Name	Address	
Bank 0 Shadow	0x00-0x01	Configures the relay of bank 0. You may configure each byte individual. Each bit corresponds to the match column. (e.g. bit 0 controls column 0) 0 – open, 1 – closed Lower Byte corresponds to the columns 0-7 Upper Byte corresponds to the columns 8-15 Power On Default: 0x00
Bank 1 Shadow	0x02-0x03	Configures the relay of bank 1. You may configure each byte individual Each bit corresponds to the match column. (e.g. bit 0 controls column 0) 0 – open, 1 – closed Lower Byte corresponds to the columns 0-7 Upper Byte corresponds to the columns 8-15 Power On Default: 0x00
Configuration	0x04	See config register bit table. Power On Default: 0x09
Readback Pointer	0x05	Sets the readback pointer. This will be read back first in an I2C read packet. Note this register will self-increment after the Host ACKnowledges at the end of each data sequence. Power On Default: 0x00

5.2.1 Bank 0 Shadow Register (0x00-0x01 Write)

This register is used to set the of the bank 0 shadow register. Each bit corresponds to the match column. (e.g. bit 0 controls column 0). It is not required to read both bytes.

When AUTO_WRITE is enabled the Bank 0 Shadow is propagated to Bank 0 register when the host send a stop condition. If AUTO_WRITE is disabled, Bank 0 Shadow will update after a general call Copy Shadow Register is issued.

Address	Bits	Description
0x00	7:0	Lower Byte corresponds to the columns 0-7
0x01	7:0	Upper Byte corresponds to the columns 8-15

5.2.2 Bank 1 Shadow Register (0x02-0x03 Write)

This register is used to set the of the bank 1 shadow register. Each bit corresponds to the match column. (e.g. bit 0 controls column 0). It is not required to read both bytes.

When AUTO_WRITE is enabled the Bank 1 Shadow is propagated to Bank 1 register when the host send a stop condition. If AUTO_WRITE is disabled, Bank 1 Shadow will update after a general call Copy Shadow Register is issued.

Address	Bits	Description
0x02	7:0	Lower Byte corresponds to the columns 0-7
0x03	7:0	Upper Byte corresponds to the columns 8-15

5.2.3 CONFIGURATION SHADOW REGISTER (0X04 WRITE)

This register is used to set Configuration Shadow Register. The table below provide a description for each bit in the register.

When AUTO_WRITE is enabled the Configuration Shadow is propagated to Configuration register when the host send a stop condition. If AUTO_WRITE is disabled, Bank 1 Shadow will update after a general call Copy Shadow Register is issued.

Name	Bits	Description
AUTO_WRITE	0	AUTO_WRITE function enable bit. When AUTO_WRITE is enabled writes into the shadow registers are propagated when a stop condition occurs. 1 – Auto write is enabled 0 – Auto write is disabled Power On Default: 1
BUS TIMEOUT FLAG CLEAR	1	Used to clear the Bus timeout flag. 1 – Clear Bus Timeout
BLOCKING MODE	2	BLOCKING_MODE function enable bit. BLOCKING_MODE function is hardware implantation to prevent more then 2 connection on a Bank at a time. 1 – Blocking mode is enabled 0 – Blocking mode is disabled Power On Default: 0
AUTO WRITE READBACK	3	AUTO_WRITE_READBACK function enable bit. When AUTO_WRITE_READBACK is enabled writes into the shadow readback register are updated immediately. 1 – Auto write readback is enabled 0 – Auto write readback is disabled Power On Default: 1
RSVD	7:4	*Reserved*

5.2.4 READBACK POINTER REGISTER (0X05 WRITE)

This register is used to set the readback pointer. The value written into this will be the first address that is return when issue a read to the controller.

Note this register will self-increment after the Host ACKnowledges at the end of each data sequence.

Bits	Description
7:0	*Reserved*

6 Troubleshooting

If you are having problems with your system, please try the following initial steps:

- **Simplify the System** – Remove modules one at a time from your system to see if there is a specific module that is causing a problem. Perform you troubleshooting with the least number of modules in the system possible.

- **Swap Components** – Try replacing parts in the system one at a time with similar parts to determine if a part is faulty or if a type of part is configured incorrectly.

If problems persist, or you have questions about configuring this product, contact RTD Embedded Technologies via the following methods:

Phone: +1-814-234-8087
E-Mail: techsupport@rtd.com

Be sure to check the RTD web site (http://www.rtd.com) frequently for product updates, including newer versions of the board manual and application software.

7 Additional Information

7.1 PC/104 Specifications

A copy of the latest PC/104 specifications can be found on the webpage for the PC/104 Embedded Consortium:

www.pc104.org

7.2 PCI and PCI Express Specification

A copy of the latest PCI and PCI Express specifications can be found on the webpage for the PCI Special Interest Group:

www.pcisig.com

8 Limited Warranty

RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD Embedded Technologies, Inc. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, RTD Embedded Technologies will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to RTD Embedded Technologies. All replaced parts and products become the property of RTD Embedded Technologies. Before returning any product for repair, customers are required to contact the factory for a Return Material Authorization (RMA) number.

This limited warranty does not extend to any products which have been damaged as a result of accident, misuse, abuse (such as: use of incorrect input voltages, improper or insufficient ventilation, failure to follow the operating instructions that are provided by RTD Embedded Technologies, “acts of God” or other contingencies beyond the control of RTD Embedded Technologies), or as a result of service or modification by anyone other than RTD Embedded Technologies. Except as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranties of merchantability and fitness for a particular purpose, and RTD Embedded Technologies expressly disclaims all warranties not stated herein. All implied warranties, including implied warranties for merchantability and fitness for a particular purpose, are limited to the duration of this warranty. In the event the product is not free from defects as warranted above, the purchaser's sole remedy shall be repair or replacement as provided above. Under no circumstances will RTD Embedded Technologies be liable to the purchaser or any user for any damages, including any incidental or consequential damages, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

Some states do not allow the exclusion or limitation of incidental or consequential damages for consumer products, and some states do not allow limitations on how long an implied warranty lasts, so the above limitations or exclusions may not apply to you.

This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

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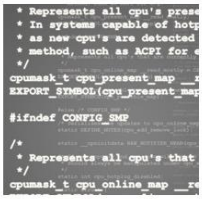

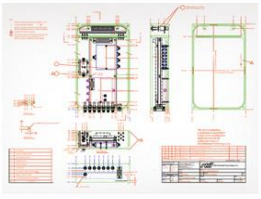

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