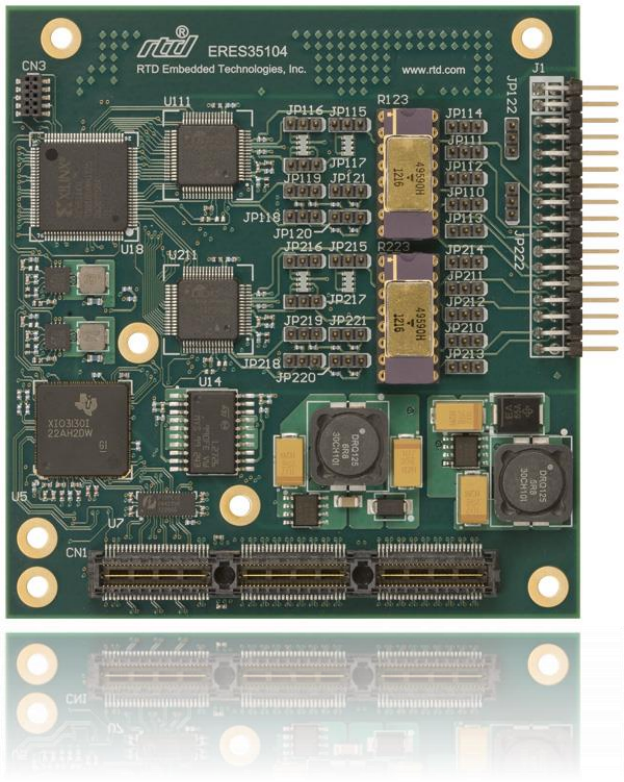
ERES35105HR

PCI Express Dual Synchro/Resolver/LVDT Interface

User's Manual

BDM-610020152 Rev. A



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Rev A	Initial Release

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1 Introduction

1.1 Product Overview

The ERES35105 provides a direct interface to two Synchro/Resolver/LVDT channels on the compact PC/104 form factor with a stackable PCI Express bus. Both sensor input channels are independently configurable with jumpers. An onboard solid state Scott-T circuitry provides a precision conversion from Synchro to Resolver signals. Onboard precision thin-film resistor divider networks for 2.0, 11.8 or 90.0 V_{RMS} configurations.

The onboard programmable sine wave oscillator reference outputs a 0 - 7V_{RMS} excitation signal with a programmable frequency range of 0 Hz to 10 kHz.

1.2 Board Features

- PC/104 form factor
- PCIe/104 stackable bus structure
  - PCIe/104 Universal Connector
  - Uses a PCIe x1 link
  - Repopulates the PCIe bus
- 2 Independent Channels
- Directly interfaces to Synchros, Resolvers and LVDTs
- Connection to 2.0V/11.8V/90.0V sensors
- Programmable resolution 10/12/14/16 - bits
- +5V only operation
- Programmable sine wave excitation
  - 0 Hz to 10 kHz frequency range
  - 0V to 7V_{RMS} voltage range
  - Up to 100mA drive current at 85C
- Dual software selectable filters can be changed on-the-fly
  - High Resolution mode for 16-bit resolution
  - High Velocity mode for tracking rate up to 320 rps
  - Other filter options available
- Synthesized reference corrects for phase shift up to 45 degrees
- Loss of signal detection
- Single-ended or Differential Inputs
- PCI Express (PCIe) x1 Upstream Interface to CPU

1.3 Ordering Information

The ERES35105 is available with the following options:

Table 1: Ordering Options

Part Number	Description
ERES35105HR-1	PCIe/104 Two-Channel, 11.8 V_{RMS} Synchro/Resolver to Digital Peripheral Module
ERES35105HR-2	PCIe/104 Two-Channel, 90.0 V_{RMS} Synchro/Resolver to Digital Peripheral Module
ERES35105HR-3	PCIe/104 Two-Channel, 2.0 V_{RMS} Synchro/Resolver to Digital Peripheral Module
IDAN- ERES35105HR-1S	PCIe/104 Two-Channel, 11.8 V_{RMS} Synchro/Resolver to Digital Peripheral Module in IDAN enclosure
IDAN- ERES35105HR-2S	PCIe/104 Two-Channel, 90.0 V_{RMS} Synchro/Resolver to Digital Peripheral Module in IDAN enclosure
IDAN- ERES35105HR-3S	PCIe/104 Two-Channel, 2.0 V_{RMS} Synchro/Resolver to Digital Peripheral Module in IDAN enclosure

The Intelligent Data Acquisition Node (IDAN™) building block can be used in just about any combination with other IDAN building blocks to create a simple but rugged 104™ stack. This module can also be incorporated in a custom-built RTD HiDAN™ or HiDANplus® High Reliability Intelligent Data Acquisition Node. Contact RTD sales for more information on our high reliability systems.

1.4 Contact Information

1.4.1 Sales Support

For sales inquiries, you can contact RTD Embedded Technologies sales via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: sales@rtd.com

1.4.2 Technical Support

If you are having problems with your system, please try the steps in the Troubleshooting section of this manual on page 28.

For help with this product, or any other product made by RTD, you can contact RTD Embedded Technologies technical support via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: techsupport@rtd.com

2 Specifications

2.1 Operating Conditions

Table 2: Operating Conditions

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{cc5}	5V Supply Voltage		4.75	5.25	V
V_{cc3}	3.3V Supply Voltage		n/a	n/a	V
V_{cc12}	12V Supply Voltage		n/a	n/a	V
V_{cc-12}	-12V Supply Voltage		n/a	n/a	V
T_a	Operating Temperature		-40	+85	C
T_s	Storage Temperature		-55	+125	C
RH	Relative Humidity	Non-Condensing	0	90%	%
MTBF	Mean Time Before Failure	Telcordia Issue 2 30°C, Ground benign, controlled		TBD	Hours

2.2 Electrical Characteristics

Table 3: Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
P	Power Consumption	V_{cc5} = 5.0V		3.5	W
I_{cc5}	5V Input Supply Current	Active		700	mA
PCIe Bus					
	Differential Output Voltage		0.8	1.2	V
	DC Differential TX Impedance		95.2	116.9	Ω
	Differential Input Voltage		0.175	3.3	V
	DC Differential RX Impedance		92.7	115.8	Ω
	Electrical Idle Detect Threshold		61	173	mV
Excitation Output (Per Channel)					
	Output Frequency		0	10k	Hz
	Output Voltage			7	V_{RMS}
	Output Current			100	mA_{RMS}
Reference Input					
	Frequency Range		0	10k	Hz
	Voltage	JPx20, JPx21 (1-2)	4.5	14.0	V_{RMS}
	Voltage	JPx20, JPx21 (2-3)	30.0	99.0	V_{RMS}
Channel Inputs					
	Frequency Range		0	10k	Hz
	Voltage (Operating)	2V Configuration	1.7	2.3	V_{RMS}
	Voltage (Operating)	11.8V Configuration	10.0	13.4	V_{RMS}
	Voltage (Operating)	90V Configuration	76.5	103.5	V_{RMS}
	Voltage (Absolute Max)	2V Configuration	-5	+5	V
	Voltage (Absolute Max)	11.8V Configuration	-30	+30	V
	Voltage (Absolute Max)	90V Configuration	-225	+225	V

3 Board Connection

NOTE: It may be necessary to disable PCIe Active State Power Management (ASPM) in the BIOS setup utility for correct operation. This is typically in the "Advanced/PCI Express/Port #" menu. Contact your CPU vendor for details.

3.1 Board Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your board in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the board at the edges, and do not touch the components or connectors. Handle the board in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

3.2 Physical Characteristics

STEP model is available upon request; contact RTD Tech Support for more information.

- Weight: Approximately 0.16 lbs. (72 g)
- Dimensions: 90.17 mm L x 95.89 mm W (3.550 in L x 3.775 in W)
- Stand-off Height: 0.600 inches (15.240 mm)

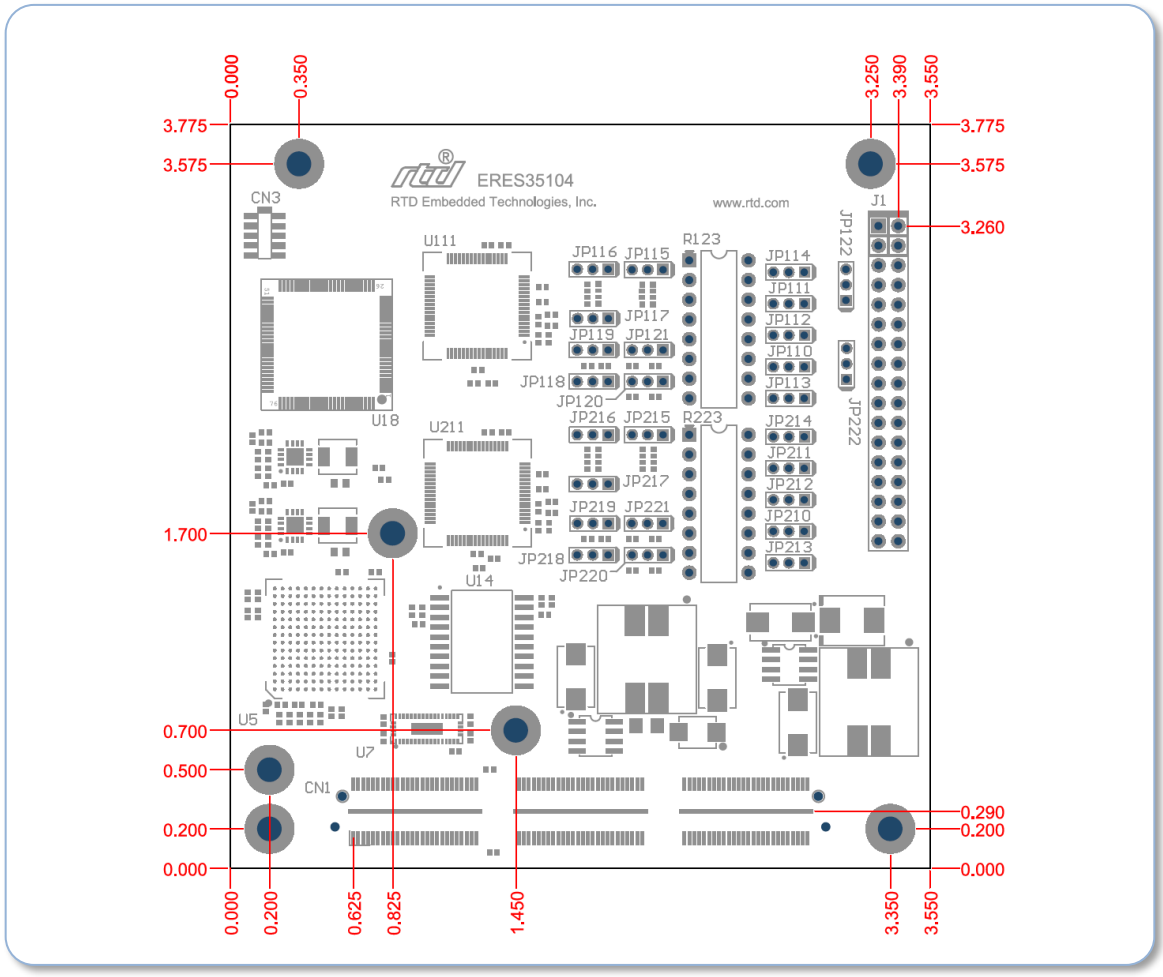

Figure 1: Board Dimensions

3.3 Connectors and Jumpers

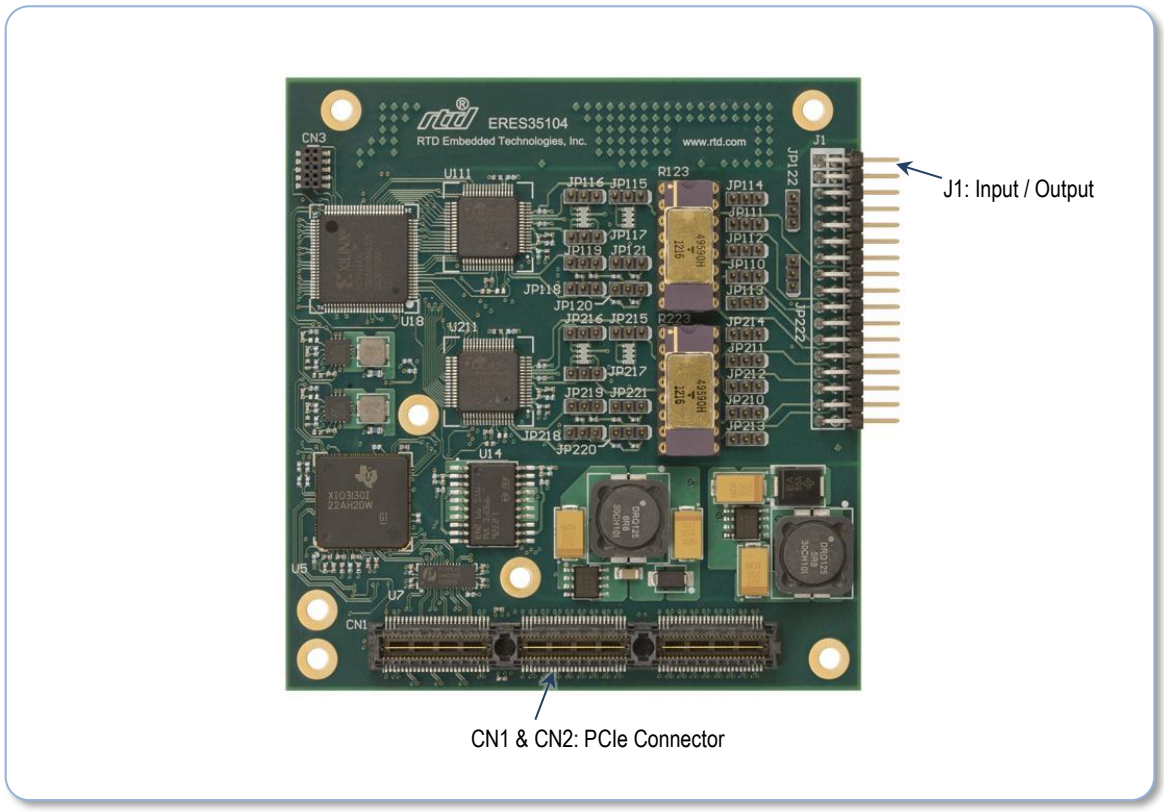

Figure 2: Board Connections

3.3.1 External I/O Connectors

J1: Sensor Input / Output

The main connector for all of the I/O is J1. It includes the connections for the Synchro/Resolver/LVDT inputs, reference inputs, excitation outputs, and some test signals. The pin assignments are shown in the Table below.

Table 4: J1 Input / Output Pin Assignments

Pin Name	#	#	Pin Name
GND	2	1	CH0_EXCITATION
GND	4	3	CH0_SINE+
GND	6	5	CH0_COSINE+
CH0_REF_IN-	8	7	CH0_REF_IN+
GND	10	9	CH1_EXCITATION
GND	12	11	CH1_SINE+
GND	14	13	CH1_COSINE+
CH1_REF_IN-	16	15	CH1_REF_IN+
CH1_VELOCITY	18	17	CH0_VELOCITY
CH0_S3	20	19	CH0_S1
CH0_S4	22	21	GND
CH0_S2_SYNCHRO	24	23	CH0_S2_RESOLVER
CH1_REF_IN+	24	25	CH0_REF_IN+
CH1_S3	28	27	CH1_S1
CH1_S4	30	29	GND
CH1_S2_SYNCHRO	32	31	CH1_S2_RESOLVER
GND	34	33	GND

3.3.2 BUS CONNECTORS

CN1 (Top) & CN2 (Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 37)

The ERES35105 is a "Universal" board, and can connect to either a Type 1 or Type 2 PCIe/104 connector.

3.3.3 JUMPERS

On all jumpers, pin 1 is designated by a thick white silkscreen line, and a square pad on the PCB. The jumpers are discussed in the following sections of this manual.

The jumper settings are described in Section 6 starting on page 21.

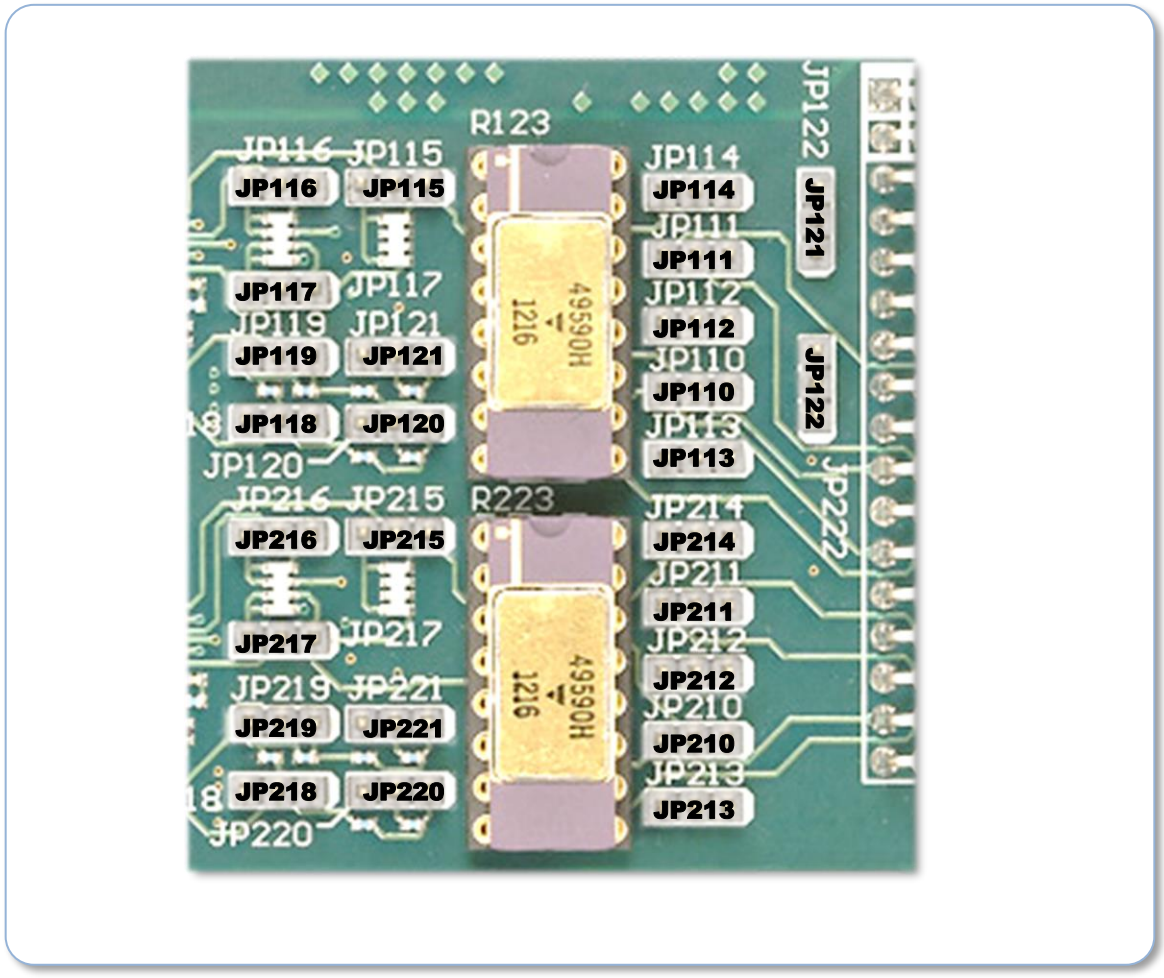

Figure 3: Jumper Locations

3.4 Steps for Installing

NOTE: It may be necessary to disable PCIe Active State Power Management (ASPM) in the BIOS setup utility for correct operation. This is typically in the "Advanced/PCI Express/Port #" menu. Contact your CPU vendor for details.

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the PC/104 system or stack.
3. Select and install stand-offs to properly position the module on the stack.
4. Remove the module from its anti-static bag.
5. Check that pins of the bus connector are properly positioned.
6. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
7. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
8. Gently and evenly press the module onto the PC/104 stack.
9. If any boards are to be stacked above this module, install them.
10. Attach any necessary cables to the PC/104 stack.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

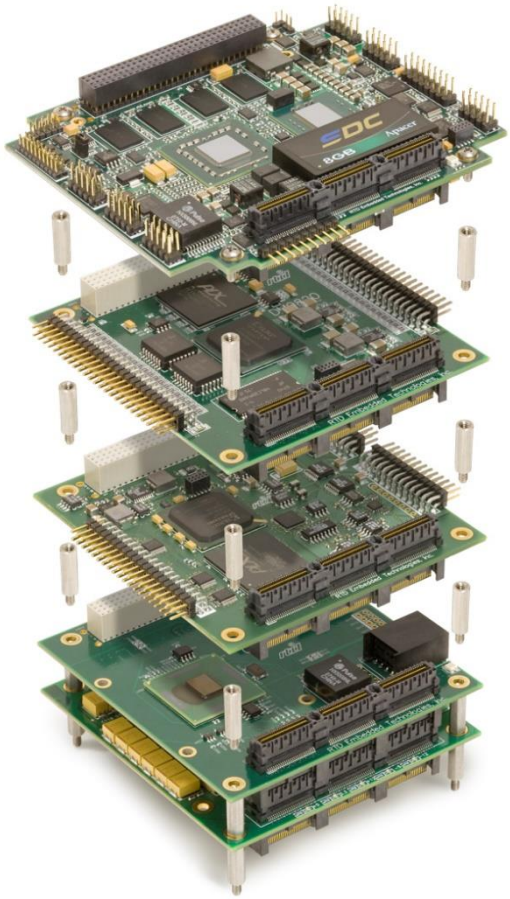

Figure 4: Example 104™ Stack

4 IDAN Connections

4.1 Module Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your module in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the module by the aluminum enclosure, and do not touch the components or connectors. Handle the module in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

4.2 Physical Characteristics

- Weight: Approximately 0.21 Kg (0.46 lbs.)
- Dimensions: 152.0 mm L x 130.0 mm W x 17.0 mm H (5.98 in L x 5.12 in W x 0.67 in H)

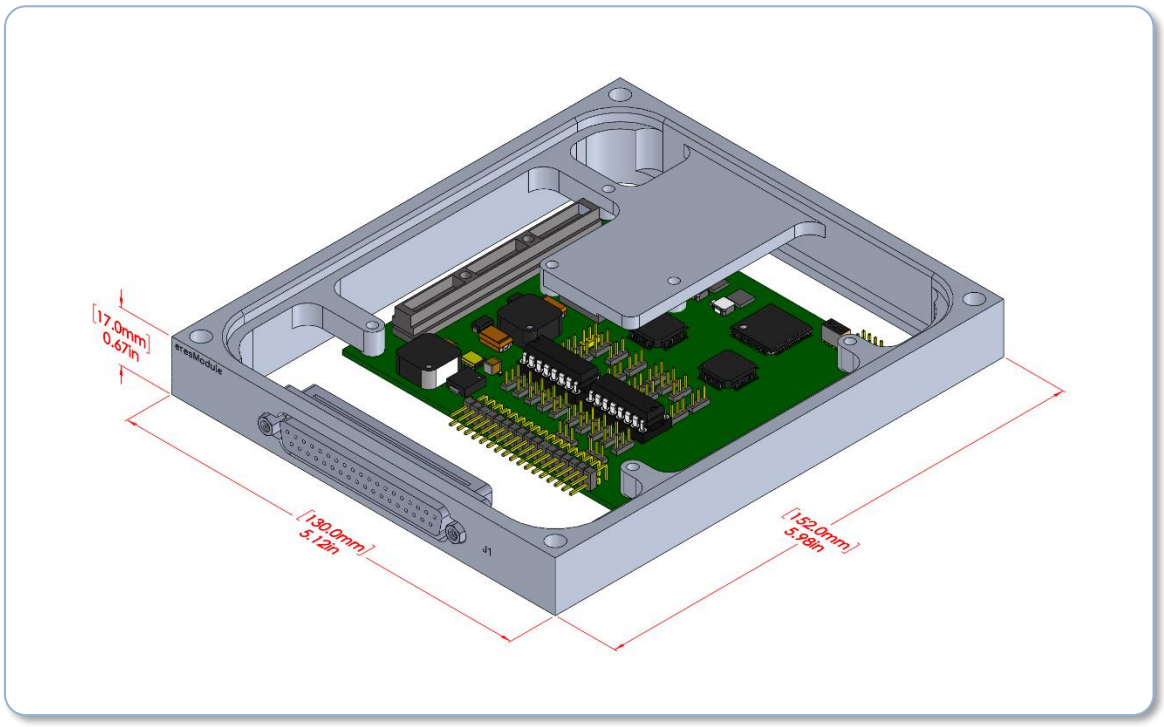

Figure 5: IDAN Dimensions

4.3 Connector Locations

The diagram below shows the connector locations for the headers of the ERES35105 as they are brought out on the front panels of the IDAN-ERES35105HR-xS. For a full description of each connector on the ERES35105, refer to the External I/O Connectors section of this manual on page 3.3.112.

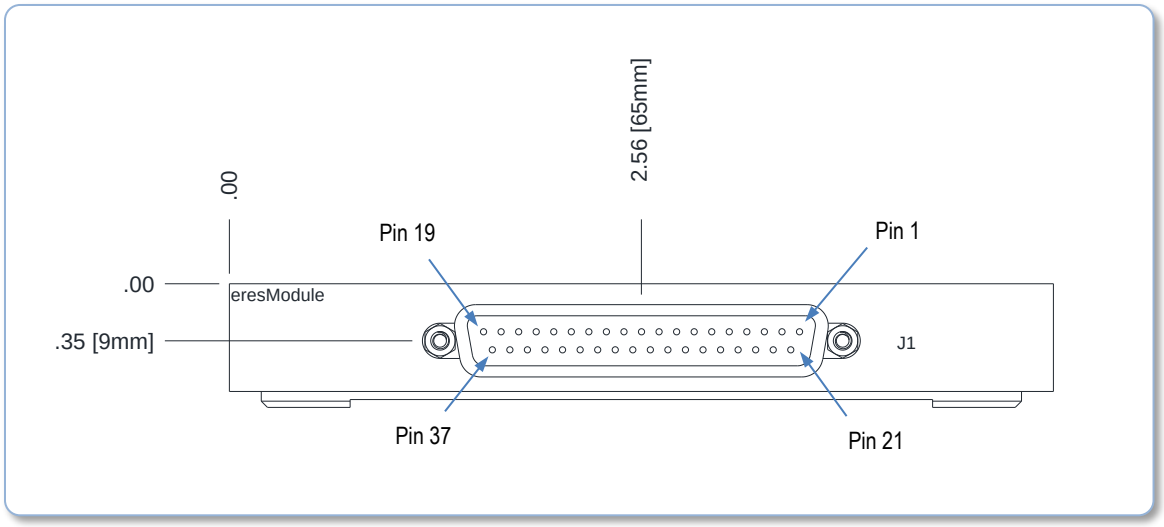

Figure 6: IDAN Front Panel Connector Locations

4.4 Connectors

Table 5: IDAN-ERES35105HR-xS Panel Connectors and Mating Connectors

Board Designator	Function	Connector Description	IDAN Panel Connector	Mating Connector
J1	Sensor Input / Output	37-pin D (socket)	AMP / TE Connectivity 1658610-1	AMP / TE Connectivity 1658608-1

4.4.1 EXTERNAL I/O CONNECTORS

Sensor Input / Output

The IDAN connector includes the connections for the Synchro/Resolver/LVDT inputs, reference inputs, excitation outputs, and some test signals. The pin assignments are shown in the Table below.

Table 6: IDAN Input / Output Pin Assignments

IDAN Pin #	Pin Name	J1 Pin #
1	CH0_EXCITATION	1
2	CH0_SINE+	3
3	CH0_COSINE+	5
4	CH0_REF_IN+	7
5	CH1_EXCITATION	9
6	CH1_SINE+	11
7	CH1_COSINE+	13
8	CH1_REF_IN+	15
9	CH0_VELOCITY	17
10	CH0_S1	19
11	GND	21
12	CH0_S2_RESOLVER	23
13	CH0_REF_IN+	25
14	CH1_S1	27
15	GND	29
16	CH1_S2_RESOLVER	31
17	GND	33
18	RESERVED	-
19	RESERVED	-
20	GND	2
21	GND	4
22	GND	6
23	CH0_REF_IN-	8
24	GND	10
25	GND	12
26	GND	14
27	CH1_REF_IN-	16
28	CH1_VELOCITY	18
29	CH0_S3	20
30	CH0_S4	22
31	CH0_S2_SYNCHRO	24
32	CH1_REF_IN+	26
33	CH1_S3	28
34	CH1_S4	30
35	CH1_S2_SYNCHRO	32
36	GND	34
37	RESERVED	-

4.4.2 BUS CONNECTORS

CN1 (Top) & CN2 (Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 37)

The ERES35105 is a "Universal" board, and can connect to either a Type 1 or Type 2 PCIe/104 connector.

4.5 Steps for Installing

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the IDAN system.
3. Remove the module from its anti-static bag.
4. Check that pins of the bus connector are properly positioned.
5. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
6. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
7. Gently and evenly press the module onto the IDAN system.
8. If any boards are to be stacked above this module, install them.
9. Finish assembling the IDAN stack by installing screws of an appropriate length.
10. Attach any necessary cables to the IDAN system.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

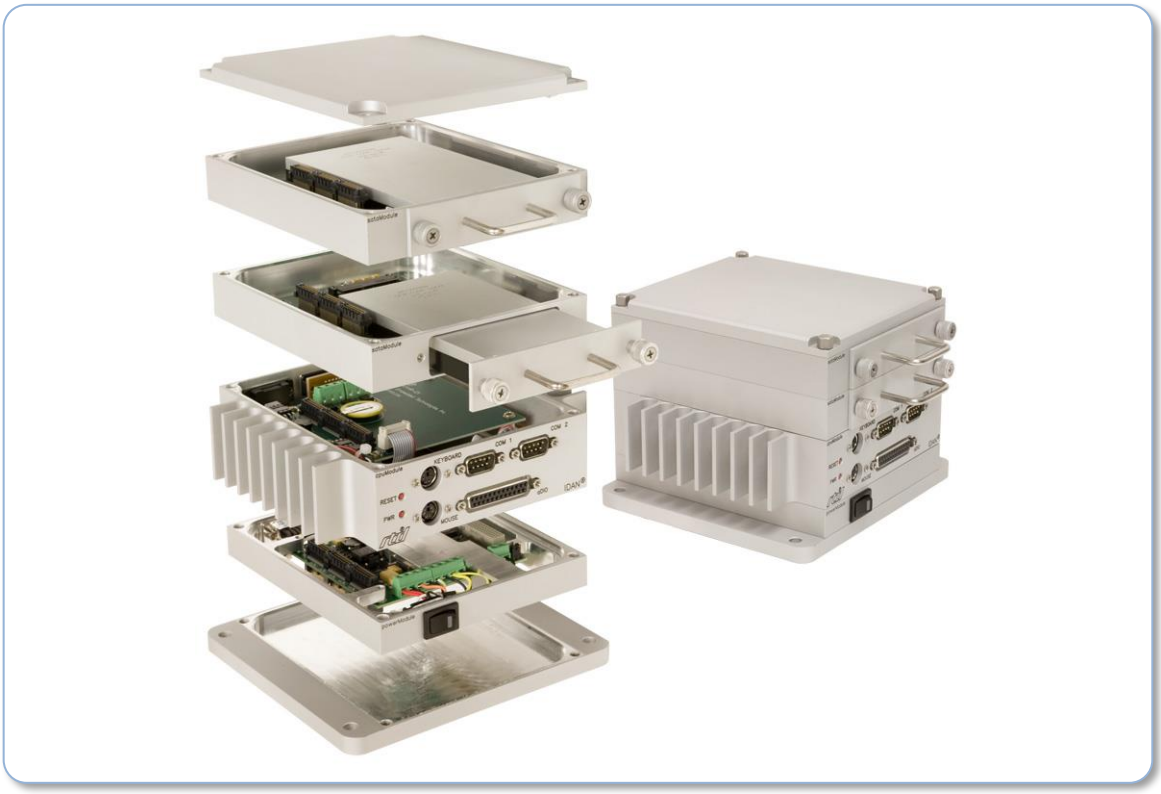

Figure 7: Example IDAN System

5 Functional Description

5.1 Block Diagram

The Figure below shows the functional block diagram of the ERES35105. The various parts of the block diagram are discussed in the following sections.

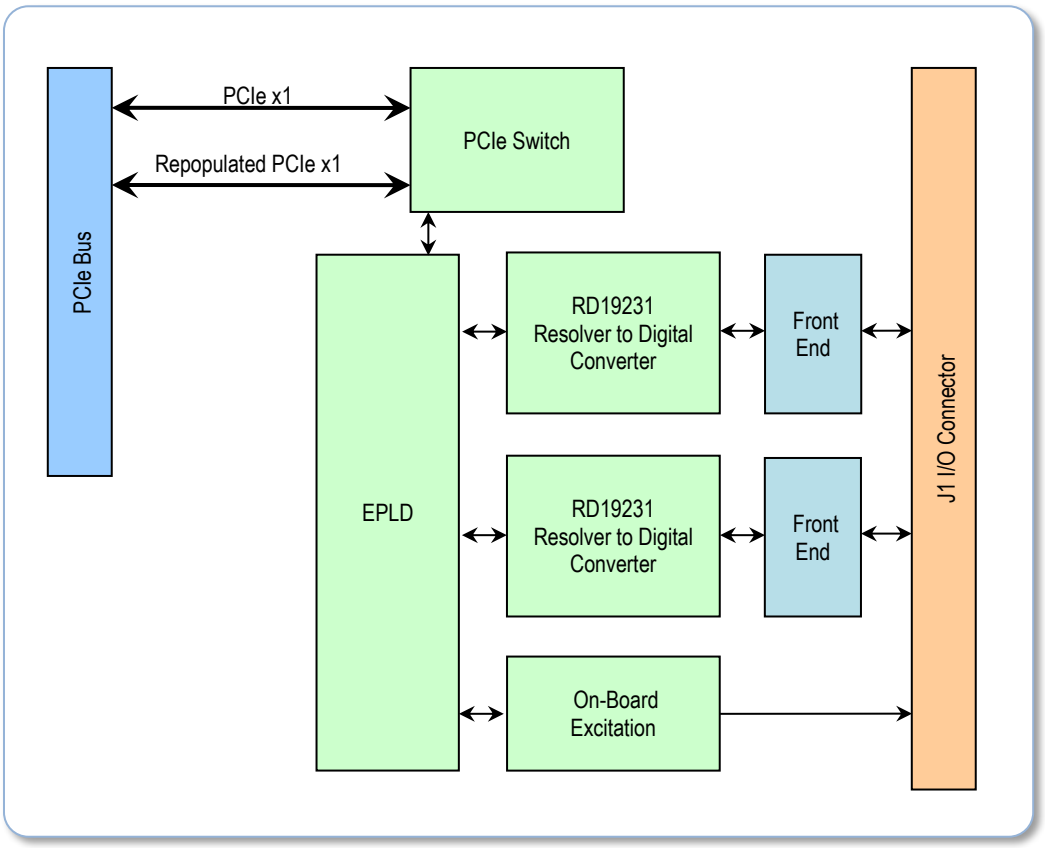

Figure 8: ERES35105 Block Diagram

5.2 PCIe Switch

The PCI Express Switch provides the bus interface to the ERES35105. The switch includes GPIO that are accessible from its Configuration Space, which is configured as a generic bus. This is a low speed interface that does not provide support for interrupts or DMA.

The PCIe Switch also provides lane repopulation. One lane is used as the uplink to the CPU. On the opposite side of the board it is replaced by a lane from the switch. This allows a virtually limitless number of boards to be added to the system.

5.3 Resolver to Digital Converter

The RD-19231 is a mixed signal CMOS IC containing analog input and digital output sections. Precision analog circuitry is merged with digital logic to form a complete high-performance tracking resolver-to-digital converter. For user flexibility and convenience, the converter bandwidth, dynamics, and velocity scaling are externally set with passive components.

The converter front-end consists of differential sine and cosine input amplifiers. The Control Transformer (CT) compares the analog input signals with the digital output, resulting in an error signal proportional to the sine of the angular difference. The CT uses a combination of amplifiers, switches, logic and capacitors in precision ratios to perform the calculation.

The converter accuracy is limited by the precision of the computing elements in the CT. Instead of a traditional precision resistor network, this converter uses capacitors with precisely controlled ratios. Sampling techniques are used to eliminate errors due to voltage drift and op-amp offsets.

The error processing is performed using the industry standard technique for Type II tracking converters. The DC error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which, together with the velocity integrator, forms a Type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above. The settings of the various error processor gains and break frequencies are done with external resistors and capacitors so that the converter loop dynamics can be easily controlled.

5.3.1 BANDWIDTH FILTERS

The Resolver to Digital Converter circuit includes two selectable bandwidth filters. The filter characteristics are shown in the Table below. For other bandwidth filter configurations, contact RTD Tech Support.

Table 7: Bandwidth Filters

Description	Filter Channel	SHIFT	Maximum Excitation Frequency	Resolution	Bandwidth	Maximum Tracking Rate
High Resolution	1	1	10 kHz	16-bit (Synchro/Resolver) 14-bit (LVDT)	180 Hz	1200 rpm
High Velocity	2	0	10 kHz	12-bit (Synchro/Resolver) 10-bit (LVDT)	750 Hz	19200 rpm

5.4 Front End

The front end consists of a precision resistor pack that sets the input voltage range (2V, 11.8V, or 90V). It also includes the jumpers to configure the board for different sensors.

Sensor signals must be converted to SIN and COS resolver signals that can be directly be interfaced by the Resolver-to-Digital converters. The classical transformer coupled connection is often too cumbersome to use. The ERES35105 module uses an operational amplifier and precision resistors to implement the Solid State Scott-T circuit. The most important design criteria in this connection are the perfect matching of the resistors. Precision is maintained by using a special trimmed resistor network together with the op-amps. These resistor networks are available for the three standard voltage levels of 2V, 11.8V and 90V. The resistor network value ratios are pre-trimmed to produce the $2V_{RMS}$ input signal required by the converters.

You may separately purchase resistor networks for the standard voltages from RTD. They may be easily configured channel-by-channel by inserting the correct resistor network into the onboard sockets. The resistor networks are used as follows:

DDC-49530 are used with 11.8V inputs
DDC-49590 are used with 90V inputs
DDC-76037 are used with 2V inputs

5.5 On-Board Excitation

The on-board excitation can be used in certain applications to provide a reference to the sensors. It consists of a Programmable Waveform Generator and two output amplifiers. Both channels must use the same excitation frequency, but the output levels can be individually adjusted.

5.6 EPLD

The EPLD provides glue logic between the PCIe interface and the on-board functions.

6 Board Configuration

6.1 Sensor Input Connections

The following sections describe how to connect and configure the ERES35105 for use with a resolver, synchro, LVDT, and direct input. All sensors except for LVDTs also require a reference input. Please see Section 6.2 on page 26 for information on connecting the reference.

6.1.1 RESOLVER INPUT

A resolver is a type of absolute rotary encoder. It consists of an excitation coil in the rotor, and two pickup coils in the stator at a 90° angle. One pickup coil has leads that are generally labeled S3 for positive and S1 for negative; and the other coil has S2 for positive and S4 for negative. This section described how to connect and configure this board for use with a resolver.

A resolver also requires a reference input. Please see Section 6.2 on page 26 for information on connecting the reference.

Input Connections

Table 8: Resolver Input Connections

Sensor		ERES35105			IDAN-ERES35105	
Lead	**Description**	**Pin Name**	**Channel 0 Pin**	**Channel 1 Pin**	**Channel 0 Pin**	**Channel 1 Pin**
S1	SINE -	CHx_S1	19	27	10	14
S2	COSINE +	CHx_S2_RESOLVER	23	31	12	16
	No Connection	CHx_S2_SYNCHRO	24	32	31	35
S3	SINE +	CHx_S3	20	28	29	33
S4	COSINE -	CHx_S4	22	30	30	34

Jumper Configuration

See Figure 3 on page 13 for jumper locations.

Table 9: Resolver Jumper Settings

Channel 0 Jumper	Channel 1 Jumper	Position
JP110	JP210	1-2
JP111	JP211	1-2
JP112	JP212	1-2
JP113	JP213	1-2
JP114	JP214	1-2
JP115	JP215	1-2
JP116	JP216	1-2
JP117	JP217	1-2
JP118	JP218	1-2

6.1.2 SYNCHRO INPUT

A synchro is a type of absolute rotary encoder. It consists of an excitation coil in the rotor, and three pickup coils in the stator at a 120° angles. The pickup coils have leads that are generally labeled S1, S2, and S3. The other ends of the coils are tied together. This section described how to connect and configure this board for use with a synchro.

A synchro also requires a reference input. Please see Section 6.2 on page 26 for information on connecting the reference.

Input Connections

Table 10: Synchro Input Connections

Sensor		ERES35105			IDAN-ERES35105	
Lead	**Description**	**Pin Name**	**Channel 0 Pin**	**Channel 1 Pin**	**Channel 0 Pin**	**Channel 1 Pin**
S1	240°	CHx_S1	19	27	10	14
	No Connection	CHx_S2_RESOLVER	23	31	12	16
S2	0°	CHx_S2_SYNCHRO	24	32	31	35
S3	120°	CHx_S3	20	28	29	33
	No Connection	CHx_S4	22	30	30	34

Jumper Configuration

See Figure 3 on page 13 for jumper locations.

Table 11: Synchro Jumper Settings

Channel 0 Jumper	Channel 1 Jumper	Position
JP110	JP210	2-3
JP111	JP211	2-3
JP112	JP212	2-3
JP113	JP213	2-3
JP114	JP214	2-3
JP115	JP215	1-2
JP116	JP216	1-2
JP117	JP217	1-2
JP118	JP218	1-2

6.1.3 2-WIRE LVDT INPUT

A 2-wire LVDT is a type of absolute linear encoder. It consists of an excitation coil and a pickup coil. There is also a moving ferromagnetic core between the two coils. The output amplitude is directly proportional to the position of the ferromagnetic core. The pickup coil has leads that are generally labeled FEEDBACK HI and FEEDBACK LO. The excitation has leads that are generally labeled REF HI and REF LO.

An LVDT does not use the reference input. It does require an excitation source that may be supplied on-board or from an external source.

An LVDT generally requires some scaling to make full use of the dynamic range of the ERES35105. In order to facilitate this, the signal path allows the addition of gain. Contact RTD Tech Support for more details.

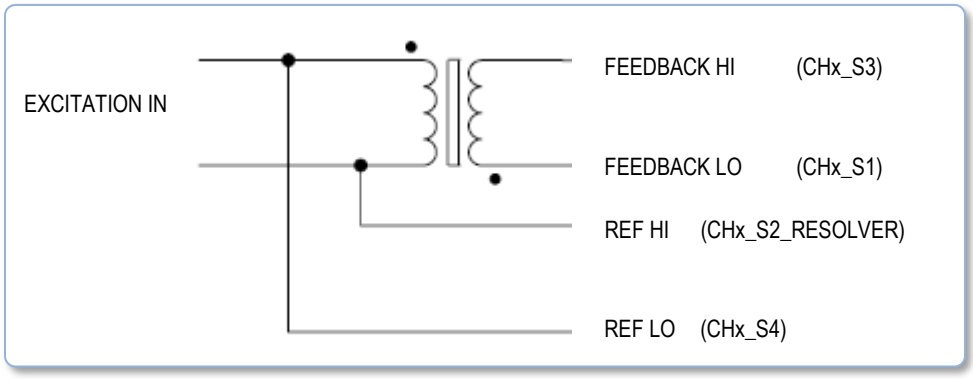

Figure 9: 2-Wire LVDT Schematic

Input Connections

Table 12: 2-Wire LVDT Input Connections

Sensor		ERES35105			IDAN-ERES35105	
Lead	Description	Pin Name	Channel 0 Pin	Channel 1 Pin	Channel 0 Pin	Channel 1 Pin
FEEDBACK LO	Pickup -	CHx_S1	19	27	10	14
REF HI	Excitation +	CHx_S2_RESOLVER	23	31	12	16
	No Connection	CHx_S2_SYNCHRO	24	32	31	35
FEEDBACK HI	Pickup +	CHx_S3	20	28	29	33
REF LO	Excitation -	CHx_S4	22	30	30	34

Jumper Configuration

See Figure 3 on page 13 for jumper locations.

Table 13: 2-Wire LVDT Jumper Settings

Channel 0 Jumper	Channel 1 Jumper	Position
JP110	JP210	1-2
JP111	JP211	1-2
JP112	JP212	1-2
JP113	JP213	1-2
JP114	JP214	1-2
JP115	JP215	2-3
JP116	JP216	2-3
JP117	JP217	2-3
JP118	JP218	2-3
JP119	JP219	2-3
JP120	JP220	Any
JP121	JP221	Any
JP122	JP222	1-2

6.1.4 3-WIRE LVDT INPUT

A 3-wire LVDT is a type of absolute linear encoder. It consists of an excitation coil and a pickup coil with a center tap. There is also a moving ferromagnetic core between the two coils. The pickup coil has leads that are generally labeled V_A, V_B, and Common.

An LVDT does not use the reference input. It does require an excitation source that may be supplied on-board or from an external source.

An LVDT generally requires some scaling to make full use of the dynamic range of the ERES35105. In order to facilitate this, the signal path allows the addition of gain. Contact RTD Tech Support for more details.

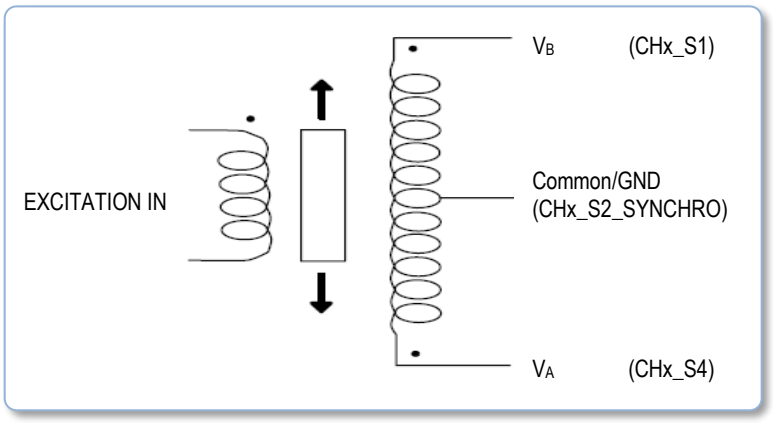

Figure 10: 3-Wire LVDT Schematic

Input Connections

Table 14: 3-Wire LVDT Input Connections

Sensor		ERES35105			IDAN-ERES35105	
Lead	Description	Pin Name	Channel 0 Pin	Channel 1 Pin	Channel 0 Pin	Channel 1 Pin
V_B	Pickup +	CHx_S1	19	27	10	14
	No Connection	CHx_S2_RESOLVER	23	31	12	16
Common	May also connect to GND	CHx_S2_SYNCHRO	24	32	31	35
	No Connection	CHx_S3	20	28	29	33
V_A	Pickup +	CHx_S4	22	30	30	34

Jumper Configuration

See Figure 3 on page 13 for jumper locations.

Table 15: 3-Wire LVDT Jumper Settings

Channel 0 Jumper	Channel 1 Jumper	Position
JP110	JP210	2-3
JP111	JP211	2-3
JP112	JP212	1-2
JP113	JP213	2-3
JP114	JP214	1-2
JP115	JP215	2-3
JP116	JP216	2-3
JP117	JP217	2-3
JP118	JP218	2-3
JP119	JP219	2-3
JP120	JP220	Any
JP121	JP221	Any
JP122	JP222	1-2

6.1.5 DIRECT INPUT

The ERES35105 also allows direct input to the resolver converter. This allows connection to other types of devices. These devices typically require a specialized external signal conditioning board.

Direct Input also requires a reference input. Please see Section 6.2 on page 26 for information on connecting the reference.

Input Connections

Table 16: Direct Input Connections

Sensor		ERES35105			IDAN-ERES35105	
Lead	**Description**	**Pin Name**	**Channel 0 Pin**	**Channel 1 Pin**	**Channel 0 Pin**	**Channel 1 Pin**
	No Connection	CHx_S1	19	27	10	14
	No Connection	CHx_S2_RESOLVER	23	31	12	16
	No Connection	CHx_S2_SYNCHRO	24	32	31	35
	No Connection	CHx_S3	20	28	29	33
	No Connection	CHx_S4	22	30	30	34
Sine	Sine Input	CHx_SINE+	3	11	2	6
Cosine	Cosine Input	CHx_COSINE+	5	13	3	7

Jumper Configuration

See Figure 3 on page 13 for jumper locations.

Table 17: Direct Input Jumper Settings

Channel 0 Jumper	Channel 1 Jumper	Position
JP110	JP210	any
JP111	JP211	any
JP112	JP212	any
JP113	JP213	any
JP114	JP214	any
JP115	JP215	Open (jumper removed)
JP116	JP216	1-2
JP117	JP217	Open (jumper removed)
JP118	JP218	1-2

6.2 Reference Input

The resolver converter requires a reference input. The reference can come from the on-board excitation signal, or from an external source. The connection to the reference is found in the following sections.

The converter uses a synthesized reference, allowing up to 45 degrees of phase shift between the reference input and the sensor inputs.

NOTE: When using in LVDT mode, the reference is derived on-board from the input signals. The CHx_REF_IN signals must be left unconnected.

6.2.1 Internally Generated Reference

Connections

Table 18: Internal Reference Connections

Sensor	ERES35105			IDAN-ERES35105	
Lead	Pin Name	Channel 0 Pin	Channel 1 Pin	Channel 0 Pin	Channel 1 Pin
REF HI	CHx_EXCITATION	1	9	1	5
REF LO	GND	2	20	22	6
No Connection	CHx_REF_IN+	7	4	15	8
No Connection	CHx_REF_IN-	8	23	16	27

Jumper Configuration

See Figure 3 on page 13 for jumper locations.

Table 19: Internal Reference Jumper Settings

Channel 0 Jumper	Channel 1 Jumper	Position
JP119	JP219	2-3
JP120	JP220	1-2
JP121	JP221	1-2
JP122	JP222	2-3

6.2.2 DIFFERENTIAL EXTERNALLY GENERATED REFERENCE

Connections

Table 20: Differential External Reference Connections

Sensor	ERES35105			IDAN-ERES35105	
Lead	Pin Name	Channel 0 Pin	Channel 1 Pin	Channel 0 Pin	Channel 1 Pin
No Connection	CHx_EXCITATION	1	9	1	5
No Connection	GND	2	20	22	6
REF HI	CHx_REF_IN+	7	15	4	8
REF LO	CHx_REF_IN-	8	16	23	27

Jumper Configuration

See Figure 3 on page 13 for jumper locations.

Table 21: Differential External Reference Jumper Settings

Channel 1 Jumper	Channel 2 Jumper	Position
JP119	JP219	1-2
JP120	JP220	2-3 ($2V_{RMS}$) 1-2 ($11.8V_{RMS}$) Open ($90V_{RMS}$)
JP121	JP221	2-3 ($2V_{RMS}$) 1-2 ($11.8V_{RMS}$) Open ($90V_{RMS}$)
JP122	JP222	1-2

6.2.3 SINGLE-ENDED EXTERNALLY GENERATED REFERENCE

Connections

Table 22: Single-Ended External Reference Connections

Sensor	ERES35105			IDAN-ERES35105	
Lead	Pin Name	Channel 0 Pin	Channel 1 Pin	Channel 0 Pin	Channel 1 Pin
No Connection	CHx_EXCITATION	1	9	1	5
No Connection	GND	2	20	22	6
REF	CHx_REF_IN+	7 or 25	15 or 26	4 or13	8 or 32
GND	GND	6	14	22	26

Jumper Configuration

See Figure 3 on page 13 for jumper locations.

Table 23: Single-Ended External Reference Jumper Settings

Channel 0 Jumper	Channel 1 Jumper	Position
JP119	JP219	2-3
JP120	JP220	2-3 ($2V_{RMS}$) 1-2 ($11.8V_{RMS}$) Open ($90V_{RMS}$)
JP121	JP221	2-3 ($2V_{RMS}$) 1-2 ($11.8V_{RMS}$) Open ($90V_{RMS}$)
JP122	JP222	1-2

7 Register Address Space

The bus interface is provided through the GPIO of the PCIe Switch. The GPIO are configured as a generic bus, and the board registers are accessed through an index and data register. The following sections describe the steps needed to access the board registers.

NOTE: It may be necessary to disable PCIe Active State Power Management (ASPM) in the BIOS setup utility for correct operation. This is typically in the "Advanced/PCI Express/Port #" menu. Contact your CPU vendor for details.

7.1 Identifying the Board

The ERES35105 shows up in standard PCI Configuration space as a set of PCI to PCI Bridges. It can be positively identified as shown in the Table below.

Table 24: Identifying the ERES35105

Configuration Space Offset	Register Description	Value
0x00	Vendor ID	0x104C
0x02	Device ID	0x8232
0x84	Subsystem Vendor ID	0x1435
0x86	Subsystem ID	0x3616

7.2 Index and Data Registers

Table 25: Index and Data Registers

Configuration Space Offset	0x03	0x02	0x01	0x00
0xBC	GPIOAB_CTRL			
0xC0	GPIOCD_CTRL			
0xC4	SELECT		INDEX_DATA	

7.2.1 GPIOAB_CTRL (READ/WRITE)

This register is used to set the direction for the GPIO port. The values to write to it are:

0x12491249 for a Write operation
0x00000000 for a Read operation

7.2.2 GPIOCD_CTRL (READ/WRITE)

This register is used to set the direction for the GPIO port. The values to write to it are:

0x01491249 for a Write operation
0x01480000 for a Read operation

7.2.3 SELECT (READ/WRITE)

This register is used to select between the Index and Data register. All undefined bits may be written with a 0.

B2: DATA
0 = Accessing Index register
1 = Accessing Data register
B1:WR_STRB
Writes take effect on 0 to 1 transition

B0: OE#

0 = Output of EPLD is enabled (for reads)
1 = Output of EPLD is disabled (for writes)

7.2.4 INDEX_DATA (READ/WRITE)

This register is used to access the Index or Data register.

NOTE: The SELECT and INDEX_DATA register may be accessed using a single 32-bit operation.

7.3 Accessing the Board Registers

7.3.1 READING FROM A BOARD REGISTER

To read one of the Board Registers, use the following steps:

1. Read the GPIOAB_CTRL, GPIOCD_CTRL, SELECT and INDEX_DATA registers and store them so they can be restored.
2. Save the Index Register
    a. Set GPIOAB_CTRL and GPIOCD_CTRL to their Read values.
    b. Set SELECT such that DATA=0, WR_STRB=0, and OE#=0
    c. Read INDEX_DATA and store it as the Old Index.
3. Set the Index Register
    a. Set SELECT such that DATA=0, WR_STRB=0, and OE#=1 and set INDEX_DATA to the desired Index.
    b. Set GPIOAB_CTRL and GPIOCD_CTRL to their Write values.
    c. Set SELECT such that DATA=0, WR_STRB=1, and OE#=1. (May also set INDEX_DATA to the desired Index again).
4. Read the Data Register
    a. Set GPIOAB_CTRL and GPIOCD_CTRL to their Read values.
    b. Set SELECT such that DATA=1, WR_STRB=0, and OE#=0
    c. Read INDEX_DATA as the desired Data.
5. Restore the Index Register
    a. Set SELECT such that DATA=0, WR_STRB=0, and OE#=1 and set INDEX_DATA to the Old Index.
    b. Set GPIOAB_CTRL and GPIOCD_CTRL to their Write values.
    c. Set SELECT such that DATA=0, WR_STRB=1, and OE#=1. (May also set INDEX_DATA to the Old Index again).
6. Restore Other Registers
    a. Restore GPIOAB_CTRL
    b. Restore GPIOCD_CTRL bit-wise or'ed with the Read Value (to make sure the SELECT pins are always output)
    c. Restore SELECT and INDEX_DATA with the WR_STRB bit cleared (to make sure a write isn't duplicated)

NOTE: If multi-thread safe operation is not required, steps 1, 2, 5, and 6 can be eliminated.

7.3.2 WRITING TO A BOARD REGISTER

To write to one of the Board Registers, use the following steps:

1. Read the GPIOAB_CTRL, GPIOCD_CTRL, SELECT and INDEX_DATA registers and store them so they can be restored.
2. Save the Index Register
    a. Set GPIOAB_CTRL and GPIOCD_CTRL to their Read values.
    b. Set SELECT such that DATA=0, WR_STRB=0, and OE#=0
    c. Read INDEX_DATA and store it as the Old Index.
3. Set the Index Register
    a. Set SELECT such that DATA=0, WR_STRB=0, and OE#=1 and set INDEX_DATA to the desired Index.
    b. Set GPIOAB_CTRL and GPIOCD_CTRL to their Write values.
    c. Set SELECT such that DATA=0, WR_STRB=1, and OE#=1. (May also set INDEX_DATA to the desired Index again).
4. Set the Data Register
    a. Set SELECT such that DATA=1, WR_STRB=0, and OE#=1 and set INDEX_DATA to the desired Data.
    b. Set GPIOAB_CTRL and GPIOCD_CTRL to their Write values. (Already set by Step 3 above)
    c. Set SELECT such that DATA=1, WR_STRB=1, and OE#=1. (May also set INDEX_DATA to the desired Data again).
5. Restore the Index Register
    a. Set SELECT such that DATA=0, WR_STRB=0, and OE#=1 and set INDEX_DATA to the Old Index.
    b. Set GPIOAB_CTRL and GPIOCD_CTRL to their Write values. (Already set by Step 3 above)
    c. Set SELECT such that DATA=0, WR_STRB=1, and OE#=1. (May also set INDEX_DATA to the Old Index again).
6. Restore Other Registers
    a. Restore GPIOAB_CTRL
    b. Restore GPIOCD_CTRL bit-wise or'ed with the Read Value (to make sure the SELECT pins are always output)
    c. Restore SELECT and INDEX_DATA with the WR_STRB bit cleared (to make sure a write isn't duplicated)

NOTE: If multi-thread safe operation is not required, steps 1, 2, 5, and 6 can be eliminated.

7.3.3 READING SHIFT REGISTER STATUS

The Index Register includes a Read-Only bit indicating whether the shift register is busy. This can be accessed as follows:

1. Read the GPIOAB_CTRL, GPIOCD_CTRL, SELECT and INDEX_DATA registers and store them so they can be restored.
2. Read the Index/Status Register
    a. Set GPIOAB_CTRL and GPIOCD_CTRL to their Read values.
    b. Set SELECT such that DATA=0, WR_STRB=0, and OE#=0
    c. Read INDEX_DATA. Bit 8 is set if the Shift Register is busy, and cleared if the Shift Register is idle.
3. Restore Other Registers
    a. Restore GPIOAB_CTRL
    b. Restore GPIOCD_CTRL bit-wise or'ed with the Read Value (to make sure the SELECT pins are always output)
    c. Restore SELECT and INDEX_DATA with the WR_STRB bit cleared (to make sure a write isn't duplicated)

NOTE: If multi-thread safe operation is not required, steps 1, and 3 can be eliminated.

7.4 Board Registers

Table 26: Board Registers

Index	Data (16-bit)
0x00	BUILD_NUM_LS
0x01	BUILD_NUM_MS
0x02	Reserved
0x03	SR_SELECT
0x04	SR_DATA_OUT
0x05	SR_DATA_IN
0x06	CH0_SETUP_STATUS
0x07	CH1_SETUP_STATUS
0x08	CH0_POSITION
0x09	CH1_POSITION

7.4.1 BUILD_NUM_LS, BUILD_NUM_MS (READ-ONLY)

These two registers contain the build number of the EPLD. It can be used to track revisions of the EPLD. BUILD_NUM_LS is the least-significant word, and BUILD_NUM_MS is the most significant word.

7.4.2 SR_SELECT (READ/WRITE)

This register selects which of the various on-board devices the shift register is accessing. Possible options are below. All other values are reserved.

0x00: Channel 0 Mode
0x01: Channel 0 Velocity Trim
0x02: Channel 1 Mode
0x03: Channel 1 Velocity Trim
0x04: Excitation Frequency
0x05: Excitation Amplitude

7.4.3 SR_DATA_OUT (READ/WRITE)

This register contains the output data for the shift register. Writing to this register also causes the shift register to start.

Prior to any writes to SR_DATA_OUT, the Shift Register Status must be checked to make sure it is idle as described in Section 7.3.3 on page 31.

7.4.4 SR_DATA_IN (READ-ONLY)

This register contains the data returned from the selected device during the last transaction.

Prior to any reads from SR_DATA_IN, the Shift Register Status must be checked to make sure it is idle as described in Section 7.3.3 on page 31.

7.4.5 CHX_SETUP_STATUS (READ/WRITE, READ-ONLY)

This register is used to setup each of the channels, and to return the status of the channels.

B0: SHIFT (Read/Write) – Selects the bandwidth filter (See Section 5.3.1 on page 20).
- 0 = Filter 2 (High Velocity)
- 1 = Filter 1 (High Resolution)

B1: DN_UP (Read/Write)
- 0 = Inactive bandwidth filter is precharged with a gain of 4. Resolution will be increased.
- 1 = Inactive bandwidth filter is precharged with a gain of ¼. Resolution will be decreased.

B2: DSR (Read/Write) – Disable Synthesized Reference
- 0 = Synthesized Reference is enabled
- 1 = Synthesized Reference is disabled

B4: DIR (Read-Only)
- 0 = Position angle is decreasing
- 1 = Position angle is increasing

B5: BIT# (Read-Only) – Built-In-Test.
- 0 = Fault condition
- 1 = No Fault condition

7.4.6 CHX_POSITION (READ-ONLY)

This register contains the current position of the sensor. A full rotation is represented as 2^{16}, regardless of number of bits. Therefore, to get the position in degrees, use the following formula:

$$\theta = \frac{(CHx_POSITION)(360)}{2^{16}}$$

If CHx_POSITION is interpreted as an unsigned integer, the range for θ is 0° to 359.99°. If CHx_POSITION is interpreted as a signed integer, the range for θ is -180° to +179.99°.

7.5 Shift Register

The shift register is used to communicate with various devices on the board. This includes digital potentiometers for setting the mode, velocity trim, and excitation amplitude, and the excitation Programmable Waveform Generator. The commands that can be sent to the devices are described in the following sections.

NOTE: Prior to any writes to SR_DATA_OUT or reads from SR_DATA_IN, the Shift Register Status must be checked to make sure it is idle as described in Section 7.3.3 on page 31.

7.5.1 Performing a Shift Register Command

To use the Shift Register, use the following steps:

1. Read the SR_SELECT board register, and store the value.
2. Wait until the Shift Register is idle (See Section 7.3.3 on page 31).
3. Write to the SR_SELECT board register with the desired device.
4. Write to the SR_DATA_OUT board register with the desired command
5. Wait until the Shift Register is idle (See Section 7.3.3 on page 31).
6. Read from the SR_DATA_IN register as the Read Data.

7.5.2 Channel x Mode (0x00 and 0x02)

This shift register select line is connected to an Intersil ISL22424 digital potentiometer. The H pin, which corresponds to a wiper value of 0xFF, is connected to +5V. The L pin, which corresponds to a wiper value of 0x00, is connected to -5V. For 0V, use a wiper value of 0x80.

Output Data

The Table below shows the value to write to the SR_DATA_OUT register to issue various commands.

Table 27: Channel Mode Shift Register

Data	Name	Description
0x60C0	Set to Non-Volatile	All subsequent writes to the wiper position are only stored in non-volatile memory. This should be done prior to adjusting the wiper, i.e. at board open.
0xC0XX	Write D0 Wiper	Writes to the wiper that is attached to the Resolver to Digital Converter D0 pin.
0xC1YY	Write D1 Wiper	Writes to the wiper that is attached to the Resolver to Digital Converter D1 pin.
0x8000	Read D0 Wiper	Reads from the wiper that is attached to the Resolver to Digital Converter D0 pin.
0x8100	Read D1 Wiper	Reads from the wiper that is attached to the Resolver to Digital Converter D1 pin.

Input Data

The lower 8 bits of the SR_DATA_IN register contain the wiper position after a read command is issued

Modes

The following table shows the values to write to the SR_DATA_OUT register to set the Resolver to Digital Converter to various modes. Each mode has two commands, one for the D0 wiper, and one for the D1 wiper. They may be written in any order.

Table 28: Channel Modes

Data	D1	D0	Mode
0xC080 0xC180	0V	0V	10-bit Synchro/Resolver
0xC0FF 0xC180	0V	5V	12-bit Synchro/Resolver
0xC080 0xC1FF	5V	0V	14-bit Synchro/Resolver
0xC0FF 0xC1FF	5V	5V	16-bit Synchro/Resolver
0xC080 0xC100	-5V	0V	8-bit LVDT
0xC000 0xC180	0V	-5V	10-bit LVDT
0xC000 0xC1FF	5V	-5V	12-bit LVDT
0xC000 0xC100	-5V	-5V	14-bit LVDT

7.5.3 Channel x Velocity Trim (0x01 and 0x03)

This shift register select line is connected to an Intersil ISL22424 digital potentiometer. Wiper 0 of the potentiometer is used to trim the velocity gain of the control loop. Wiper 1 of the potentiometer is used to trim the velocity offset of the control loop. Velocity trimming is only required when using the analog CHx_VELOCITY outputs.

Output Data

The Table below shows the value to write to the SR_DATA_OUT register to issue various commands.

Table 29: Velocity Trim Shift Register

Data	Name	Description
0x60C0	Set to Non-Volatile	All subsequent writes to the wiper position are only stored in non-volatile memory. This should be done prior to adjusting the wiper, i.e. at board open.
0xC0XX	Write Gain Trim Wiper	A value of 0x00 is minimum gain, 0x80 is nominal, and 0xFF is maximum gain.
0xC1YY	Write Offset Trim Wiper	A value of 0x00 is most negative offset, 0x80 is nominal, and 0xFF is most positive offset.
0x8000	Read Gain Trim Wiper	Reads the current wiper position.
0x8100	Read Offset Trim Wiper	Reads the current wiper position.

Input Data

The lower 8 bits of the SR_DATA_IN register contain the wiper position after a read command is issued

7.5.4 EXCITATION FREQUENCY (0X04)

This shift register select line is connected to an Analog Devices AD9833 Programmable Waveform Generator. This Generator uses a 28-bit phase accumulator based on a 20 MHz clock. To calculate the value to write to the 28-bit FREQ register, use the following formula:

$$FREQ = \frac{(Frequency)(2^{28})}{20\ MHz}$$

Output Data

To set the output frequency, several writes to SR_DATA_OUT are required. These must be performed in order. In this list, the pipe represents a bit-wise or operation, and the square brackets represent the bits in the FREQ register.

1. 0x2000
2. 0x4000 | FREQ[13:0]
3. 0x4000 | FREQ[27:14]

Input Data

The Programmable Waveform Generator does not provide any read data.

7.5.5 EXCITATION AMPLITUDE (0X05)

This shift register select line is connected to an Intersil ISL22424 digital potentiometer. Wiper 0 of the potentiometer is used to adjust the amplitude of the Channel 0 Excitation. Wiper 1 of the potentiometer is used to adjust the amplitude of the Channel 1 Excitation.

Output Data

The Table below shows the value to write to the SR_DATA_OUT register to issue various commands.

Table 30: Excitation Amplitude Shift Register

Data	Name	Description
0x60C0	Set to Non-Volatile	All subsequent writes to the wiper position are only stored in non-volatile memory. This should be done prior to adjusting the wiper, i.e. at board open.
0xC0XX	Write Channel 0 Wiper	Output amplitude. See Table 30 below. Values may be interpolated.
0xC1YY	Write Channel 1 Wiper	Output amplitude. See Table 30 below. Values may be interpolated.
0x8000	Read Channel 0 Wiper	Reads the current wiper position.
0x8100	Read Channel 1 Wiper	Reads the current wiper position.

Table 31: Excitation Amplitude Values

Value	Amplitude (V_{RMS})	Amplitude (V_{P-P})
0x00	0.0	0.0
0x3B	2.0	5.7
0x95	5.0	14.1
0xD1	7.0	19.8

Input Data

The lower 8 bits of the SR_DATA_IN register contain the wiper position after a read command is issued.

8 Troubleshooting

NOTE: It may be necessary to disable PCIe Active State Power Management (ASPM) in the BIOS setup utility for correct operation. This is typically in the "Advanced/PCI Express/Port #" menu. Contact your CPU vendor for details.

If you are having problems with your system, please try the following initial steps:

- **Simplify the System** – Remove modules one at a time from your system to see if there is a specific module that is causing a problem. Perform you troubleshooting with the least number of modules in the system possible.

- **Swap Components** – Try replacing parts in the system one at a time with similar parts to determine if a part is faulty or if a type of part is configured incorrectly.

If problems persist, or you have questions about configuring this product, contact RTD Embedded Technologies via the following methods:

Phone: +1-814-234-8087
E-Mail: techsupport@rtd.com

Be sure to check the RTD web site (http://www.rtd.com) frequently for product updates, including newer versions of the board manual and application software.

9 Additional Information

9.1 PC/104 Specifications

A copy of the latest PC/104 specifications can be found on the webpage for the PC/104 Embedded Consortium:

www.pc104.org

9.2 PCI and PCI Express Specification

A copy of the latest PCI and PCI Express specifications can be found on the webpage for the PCI Special Interest Group:

www.pcisig.com

10 Limited Warranty

RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD Embedded Technologies, Inc. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, RTD Embedded Technologies will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to RTD Embedded Technologies. All replaced parts and products become the property of RTD Embedded Technologies. Before returning any product for repair, customers are required to contact the factory for a Return Material Authorization (RMA) number.

This limited warranty does not extend to any products which have been damaged as a result of accident, misuse, abuse (such as: use of incorrect input voltages, improper or insufficient ventilation, failure to follow the operating instructions that are provided by RTD Embedded Technologies, “acts of God” or other contingencies beyond the control of RTD Embedded Technologies), or as a result of service or modification by anyone other than RTD Embedded Technologies. Except as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranties of merchantability and fitness for a particular purpose, and RTD Embedded Technologies expressly disclaims all warranties not stated herein. All implied warranties, including implied warranties for merchantability and fitness for a particular purpose, are limited to the duration of this warranty. In the event the product is not free from defects as warranted above, the purchaser's sole remedy shall be repair or replacement as provided above. Under no circumstances will RTD Embedded Technologies be liable to the purchaser or any user for any damages, including any incidental or consequential damages, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

Some states do not allow the exclusion or limitation of incidental or consequential damages for consumer products, and some states do not allow limitations on how long an implied warranty lasts, so the above limitations or exclusions may not apply to you.

This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

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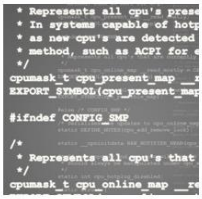

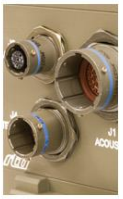
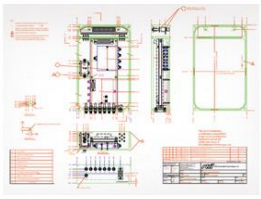

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