FPGA35S6046HR

FPGA35S6101HR

FPGA Module

User's Manual

BDM-610010048 Rev. C

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AS9100 and ISO 9001 Certified

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Revision History

Rev A	Initial Release
Rev B	Updated pictures. Added User ID jumpers. Added configuration flash, PCI vendor and device ID.
Rev C	Changed Solder jumper from B1 to B2 in sections 3.3.1 and 4.3.3

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1 Introduction

1.1 Product Overview

The FPGA35S6 series of FPGA boards are designed to provide a platform to create any digital I/O that is required for your application. It interfaces with the PCIe bus and features a Xilinx Spartan 6 FPGA with a 27 MHz oscillator and 1Gb of DDR2 SDRAM. The FPGA35S6046 and FPGA35S6101 provide 32 RS-232/422/485 I/O, 24 5V tolerant I/O and 40 3.3V tolerant high speed I/O.

1.2 Board Features

- Xilinx Spartan 6 System level features
  - XC6SLX45T (FPGA35S6046HR)
    - 43,661 Logic Cells
    - 2,489 kb of internal RAM
      - 116 18Kb (2088 Kb Max) Block RAM
      - 401 kB Distributed RAM
    - XCF16PFSG48C Configuration Flash
  - XC6SLX100T (FPGA35S6101HR)
    - 101,261 Logic Cells
    - 5,800 kb of internal RAM
      - 268 18Kb (4,824 Kb Max) Block RAM
      - 976 kB Distributed RAM
    - XCF32PFSG48C Configuration Flash
  - RAM hierarchical memory:
    - Each block RAM has two independent ports
    - Programmable Data Width
  - Integrated Endpoint block for PCI Express
  - Integrated Memory Controller
    - 1 Gb of DDR2 SDRAM
    - Supports access rates of up to 800Mb/s
  - Dedicated carry logic for high-speed arithmetic
  - Abundant logic resources with increased logic capacity
    - Optional shift register or distributed RAM support
    - Efficient 6-input LUTs
    - LUT with dual flip-flops
  - Four dedicated DLLs for advanced clock control
    - Phase shift input clock by 0, 90, 180, 270
    - Multiply input clock by 2 to 32
    - Divide input clock by 1 to 32
- Digital I/O Connectors
  - 32 RS-232/422/485 I/O
    - Four connectors
    - Exar SP338EER1-L Transceivers
    - Each connector can support a single full RS-232 port or two TX/RX only ports
    - Up to 1 Mbps in RS-232 mode
    - Up to 20 Mbps in RS-422/485 mode
    - ESD Protected
  - 24 5V tolerant Digital I/O
    - Selectable pull-up/pull-down per byte
    - Pull-up can be 3.3V or 5V
    - ESD Protected
    - Can be used as LVDS Input/Output or LVTTL Input/Output
  - 40 3.3V tolerant High-Speed I/O
    - ESD Protected
    - Can be used as LVDS Input or LVTTL Input/Output
- Fully supported by Xlinx development system
  - ISE WebPACK (free download from http://www.xilinx.com)
  - ISE Design Suite
- Embedded Digilent® USB JTAG Programmer
  - Allows programming from the host computer

- Compatible with Xilinx tools, including iMpact and ChipScope
- PCI Express Bus:
  - PCIe/104 Universal Board
    - Interfaces with Type 1 or Type 2 bus
    - No re-population
  - Provides 2.5 Gbps in each direction
  - In-band interrupts and messages
  - Message Signaled Interrupt (MSI) support

1.3 Ordering Information

The FPGA35S6 series of FPGA boards is available in the following options:

Table 1: Ordering Options

Part Number	Description
FPGA35S6046HR	PCIe/104 Spartan-6 XC6SLX45T User Programmable FPGA Module
FPGA35S6101HR	PCIe/104 Spartan-6 XC6SLX100T User Programmable FPGA Module
IDAN-FPGA35S6046HR	PCIe/104 Spartan-6 XC6SLX45T User Programmable FPGA Module in IDAN enclosure
IDAN-FPGA35S6101HR	PCIe/104 Spartan-6 XC6SLX100T User Programmable FPGA Module in IDAN enclosure

A Starter Kit is available for any of the options, which includes the appropriate programming cable. Contact RTD Sales for more information.

The FPGA35S6 is a general use FPGA module, allowing you to design your own FPGA. It has support for custom oscillator and larger Xilinx Spartan 6 FPGAs. Please contact RTD Embedded Technologies for more information on custom FPGA35S6 products and custom FPGA designs.

The Intelligent Data Acquisition Node (IDAN™) building block can be used in just about any combination with other IDAN building blocks to create a simple but rugged 104™ stack. This module can also be incorporated in a custom-built RTD HiDAN™ or HiDANplus High Reliability Intelligent Data Acquisition Node. Contact RTD sales for more information on our high reliability systems.

1.4 Contact Information

1.4.1 Sales Support

For sales inquiries, you can contact RTD Embedded Technologies sales via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: sales@rtd.com

1.4.2 Technical Support

If you are having problems with you system, please try the steps in the Troubleshooting section of this manual.

For help with this product, or any other product made by RTD, you can contact RTD Embedded Technologies technical support via the following methods:

Phone: 1-814-234-8087 Monday through Friday, 8:00am to 5:00pm (EST).
E-Mail: techsupport@rtd.com

2 Specifications

2.1 Operating Conditions

Table 2: Operating Conditions

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{cc5}	5V Supply Voltage		4.75	5.25	V
V_{cc3}	3.3V Supply Voltage		n/a	n/a	V
V_{cc12}	12V Supply Voltage		n/a	n/a	V
T_a	Operating Temperature		-40	+85	C
T_s	Storage Temperature		-40	+85	C
RH	Relative Humidity	Non-Condensing	0	90%	%
MTBF	Mean Time Before Failure	Telcordia Issue 2 30°C, Ground benign, controlled		TBD	Hours

2.2 Electrical Characteristics

Table 3: Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
P	Power Consumption(1)	V_{cc5} = 5.0V		2.5		W
I_{cc}	5V Input Supply Current(1)	Active		500		mA
	PCIe/104 Bus					
	Differential Output Voltage		0.8		1.2	V
	DC Differential TX Impedance		80		120	Ω
	Differential Input Voltage		0.175		1.2	V
	DC Differential RX Impedance		80		120	Ω
	Electrical Idle Detect Threshold		65		175	mV
	Serial Transceivers					
V_{IH}	Input High Voltage	RS-232 mode	2.0	1.5	+15	V
V_{IL}	Input Low Voltage	RS-232 mode	-15	1.2	0.6	V
V_{OH}	Output High Voltage	RS-232 mode	5.0	5.5	7.0	V
V_{OL}	Output Low Voltage	RS-232 mode	-7.0	-5.5	-5.0	V
V_{TH}	Input Differential Threshold	RS-422/485 mode	-200	-125	-50	mV
R_{IN}	Input Resistance	RS-422/485 mode TERM = 0 -7V ≤ V_{IN} ≤ 12V	96			kΩ
R_{TERM}	Termination Resistance	RS-422/485 mode TERM = 1 -7V ≤ V_{IN} ≤ 12V	100	120	155	Ω
V_{OD}	Output Differential Voltage	RS-422/485 mode R_L=100Ω (RS-422) R_L=54Ω (RS-485)	 2.0 1.5			V
V_{CM}	Driver Common Mode Output Voltage	RS-422/485 mode			3.0	V
	Digital I/O					
V_{IH}	Input High Voltage	CN9	2.0		5.5	V
V_{IH}	Input High Voltage	CN8	2.0		3.6	V
V_{IL}	Input Low Voltage	CN8,CN9	-0.5		0.8	V
V_{OH}	Output High Voltage	I_O = -12mA CN8,CN9	2.6		3.3	V
V_{OL}	Output Low Voltage	I_O = 12mA CN8,CN9	0		0.4	V
	5V Output	CN8,CN9			200	mA
	DDR2 Interface					
	Access Rate(2)		250		800	Mb/s

Note: (1): Typical power consumption based on RTD's FPGA example.
(2): Proving by design, not production tested.

For additionally electrical characteristic of the Spartan 6 I/O refer to http://www.xilinx.com

3 Board Connection

3.1 Board Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your board in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the board at the edges, and do not touch the components or connectors. Handle the board in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

3.2 Physical Characteristics

- Weight: Approximately 63.5 g (0.14 lbs.)
- Dimensions: 90.17 mm L x 95.89 mm W (3.550 in L x 3.775 in W)

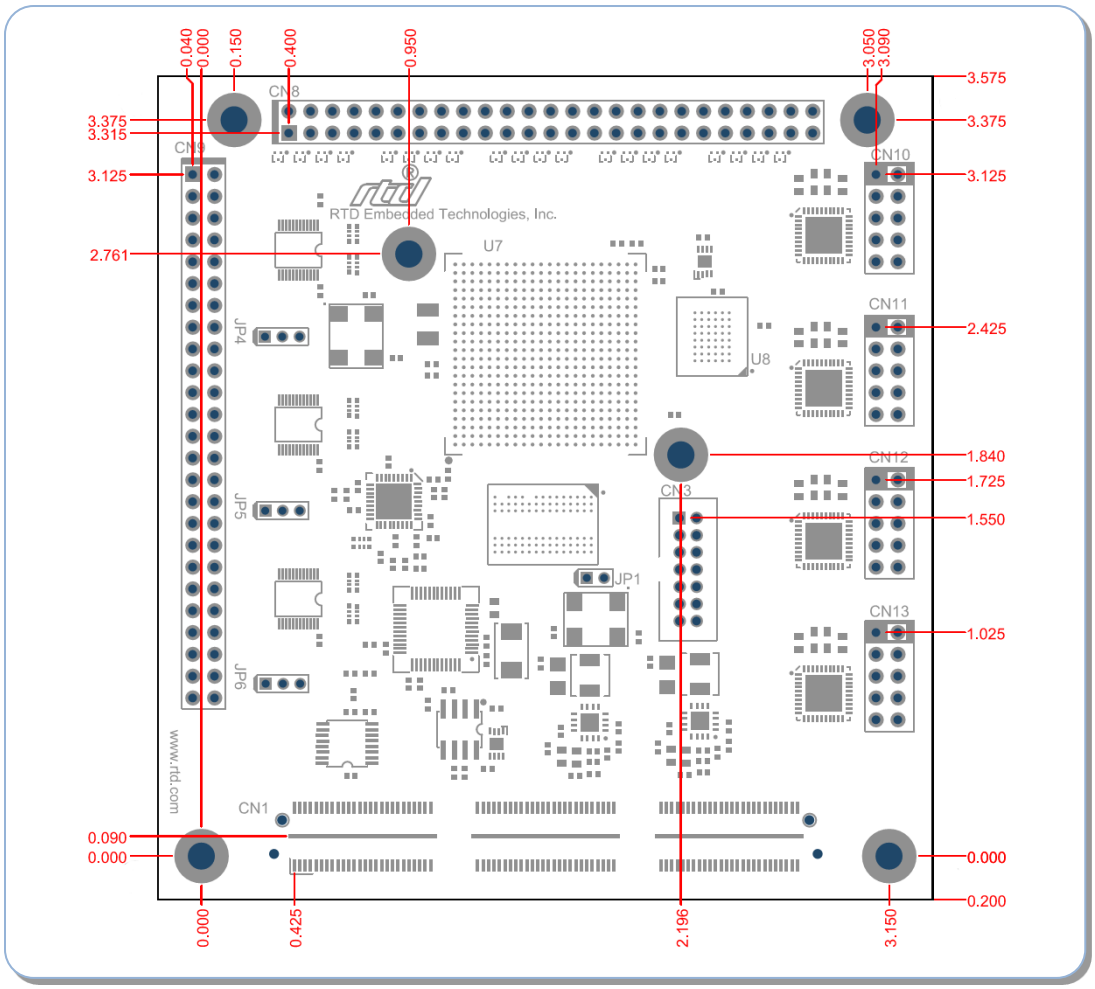

Figure 1: Board Dimensions

3.3 Connectors and Jumpers

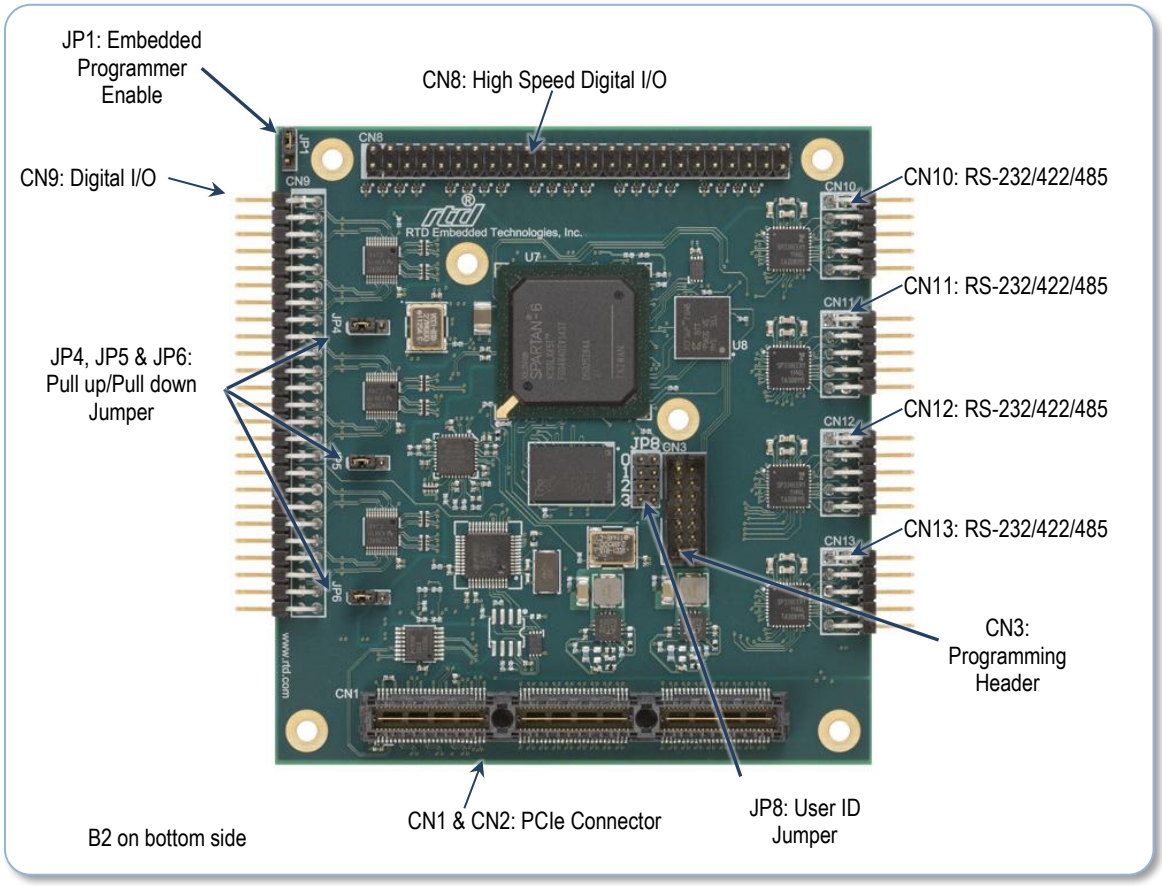

Figure 2: Board Connections

3.3.1 External I/O Connectors

CN3: Xilinx JTAG Programming Header

Connector CN3 provides a connection to the Xilinx JTAG programming header. The pin assignment for CN3 is shown below. This connector header mates with the Xilinx OEM programming cable.

Table 4: CN3 Programming Header

3.3V VRef	2	1	GND
TMS	4	3	GND
TCK	6	5	GND
TDO	8	7	GND
TDI	10	9	GND
N/C	12	11	GND
N/C	14	13	GND

CN8: High Speed Digital I/O Connector

Connector CN8 provides 40 digital I/O lines, along with a +5V pin and ground pins. These signals are 3.3V tolerant. The signal names reflect the signal names I n the Xilinx UCF file with the device pin out.

CN8 is attached to Bank 1, and supports any of the Spartan 6 I/O Standards that use a 3.3V V_{CCO} and no reference voltage. This includes LVTTL, LVCMOS33 input and output, and LVDS_33 input. LVDS output is not supported in Bank 1.

Table 5: CN8 I/O Pin Assignments

Port2_n[0]	2	1	Port2_p[0]
Port2_n[1]	4	3	Port2_p[1]
Port2_n[2]	6	5	Port2_p[2]
Port2_n[3]	8	7	Port2_p[3]
GND	10	9	GND
Port2_n[4]	12	11	Port2_p[4]
Port2_n[5]	14	13	Port2_p[5]
Port2_n[6]	16	15	Port2_p[6]
Port2_n[7]	18	17	Port2_p[7]
GND	20	19	GND
Port2_n[8]	22	21	Port2_p[8]
Port2_n[9]	24	23	Port2_p[9]
Port2_n[10]	26	25	Port2_p[10]
Port2_n[11]	28	27	Port2_p[11]
GND	30	29	GND
Port2_n[12]	32	31	Port2_p[12]
Port2_n[13]	34	33	Port2_p[13]
Port2_n[14]	36	35	Port2_p[14]
Port2_n[15]	38	37	Port2_p[15]
GND	40	39	GND
Port2_n[16]	42	41	Port2_p[16]
Port2_n[17]	44	43	Port2_p[17]
Port2_n[18]	46	45	Port2_p[18]
Port2_n[19]	48	47	Port2_p[19]
GND	50	49	+5V

CN9: Digital I/O Connector

Connector CN9 provides 24 digital I/O lines, along with a +5V pin and ground pins. All I/O have pull up/pull down resistors that are controlled by jumper options, also shown in the table. These signals are 5V tolerant. The signal names reflect the signal names in the Xilinx UCF file with the device pin out.

CN9 is attached to Bank 0, and supports any of the Spartan 6 I/O Standards that use a 3.3V V_{CCO} and no reference voltage. This includes LVTTL, LVCMOS33, and LVDS_33 input and output.

Table 6: CN9 I/O Pin Assignments

GND	2	1	port1_p[0]	JP4
GND	4	3	port1_n[0]	
GND	6	5	port1_p[1]	
GND	8	7	port1_n[1]	
GND	10	9	port1_p[2]	
GND	12	11	port1_n[2]	
GND	14	13	port1_p[3]	
GND	16	15	port1_n[3]	
GND	18	17	port1_p[4]	JP5
GND	20	19	port1_n[4]	
GND	22	21	port1_p[5]	
GND	24	23	port1_n[5]	
GND	26	25	port1_p[6]	
GND	28	27	port1_n[6]	
GND	30	29	port1_p[7]	
GND	32	31	port1_n[7]	JP6
GND	34	33	port1_p[8]	
GND	36	35	port1_n[8]	
GND	38	37	port1_p[9]	
GND	40	39	port1_n[9]	
GND	42	41	port1_p[10]	
GND	44	43	port1_n[10]	
GND	46	45	port1_p[11]	
GND	48	47	port1_n[11]	
GND	50	49	+5V	

CN10, CN11, CN12, CN13: RS-232/422/485 Transceiver Connectors

These connectors each provide configurable RS-232/422/485 transceivers. The pin configuration and associated FPGA signals are shown in the Table below. For other modes, and information on how to configure the port, see Section 5.7 on page 25. The signal names reflect the signal names in the Xilinx UCF file with the device pin out.

CN10 is associated with the “com1” signals, CN11 with the “com2” signals, CN12 with the “com3” signals, and CN13 with the “com4” signals. These signals are attached to Bank 2 of the FPGA, and should be configured as LVCMOS33.

Table 7: CN10, CN11, CN12, CN13 I/O Pin Assignments

com?_dsr (RX)	2	1	com?_dcd (RX)
com?_rtd (TX)	4	3	com?_rxd (RX)
com?_cts (RX)	6	5	com?_txd (TX)
com?_ri (RX)	8	7	com?_dtr (TX)
GND	10	9	GND

3.3.2 BUS CONNECTORS

CN1(Top) & CN2(Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 35)

The FPGA35S6 is a "Universal" board, and can connect to either a Type 1 or Type 2 PCIe/104 connector.

3.3.3 JUMPERS

JP4, JP5, JP6: Pull up/Pull down Jumper

JP4, JP5, and JP6 are 3-pin two position jumpers that are used to set pull up or pull downs options on the I/O signal lines of CN9. Refer to Table 6 to determine which I/O pins are effected by each jumper.

Table 8: Pull up/Pull down Jumper options

Setting	Description
1-2	I/O is pulled up to 3.3V or 5V (Set by B1 and B2)
2-3	I/O is pulled down to GND
No Jumper	I/O has no pull up/pull down

JP1: Embedded Programmer Enable

This jumper is used to enable the embedded programmer to the JTAG chain. See Section 5.8 on page 26 for more details. The board can be programmed from and external programmer with this jumper in either position.

Table 9: JP1 – Embedded Programmer Enable

Setting	Description
1-2	Enabled embedded programmer
2-3 or open	Disables embedded programmer

JP8: User ID Jumper

The User ID Jumper is a four position, user defined jumper block. The jumpers can be read by the FPGA. An installed jumper results in a logic low, and an open jumper results in a logic high.

Table 10: JP8 – User ID Jumper

Position	Description
1-2	User ID bit 0
3-4	User ID bit 1
5-6	User ID bit 2
7-8	User ID bit 3

3.3.1 SOLDER JUMPER

B2: Pull up Voltage

Solder jumper B2 is used to set the pull up voltage for JP4, JP5 and JP6.

Table 11: B2 Pull up Voltage

Setting	Description
1-2	Sets Pull up voltage to 3.3V
2-3	Sets Pull up voltage to 5V

3.4 Steps for Installing

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the PC/104 system or stack.
3. Select and install stand-offs to properly position the module on the stack.
4. Remove the module from its anti-static bag.
5. Check that pins of the bus connector are properly positioned.
6. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
7. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
8. Gently and evenly press the module onto the PC/104 stack.
9. If any boards are to be stacked above this module, install them.
10. Attach any necessary cables to the PC/104 stack.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

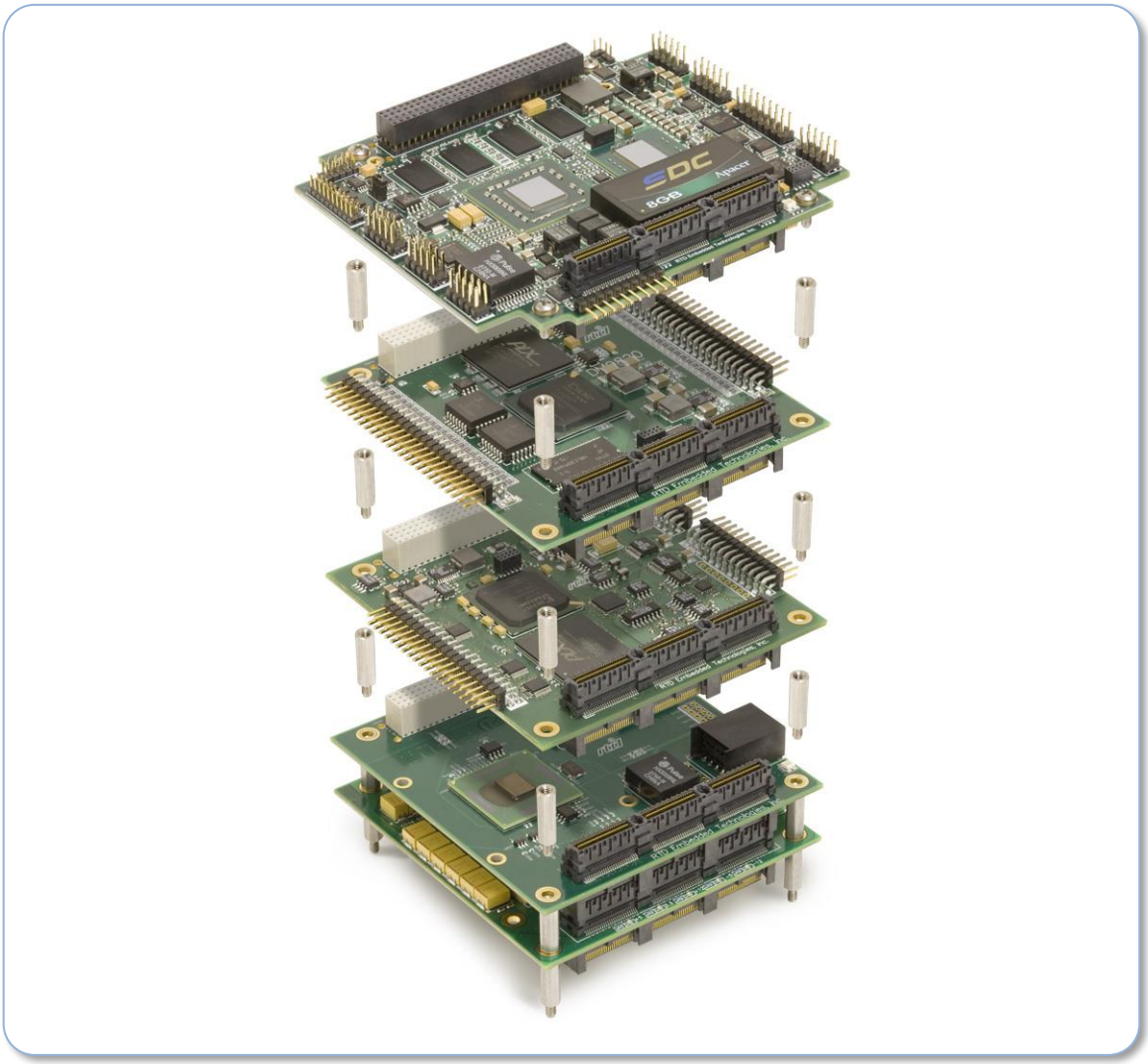

Figure 3: Example 104™ Stack

4 IDAN Connections

4.1 Module Handling Precautions

To prevent damage due to Electrostatic Discharge (ESD), keep your module in its antistatic bag until you are ready to install it into your system. When removing it from the bag, hold the module by the aluminum enclosure, and do not touch the components or connectors. Handle the module in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

4.2 Physical Characteristics

- Weight: Approximately 0.42 Kg (0.92 lbs.)
- Dimensions: 152mm L x 130mm W x 34mm H (5.983" L x 5.117" W x 1.339" H)

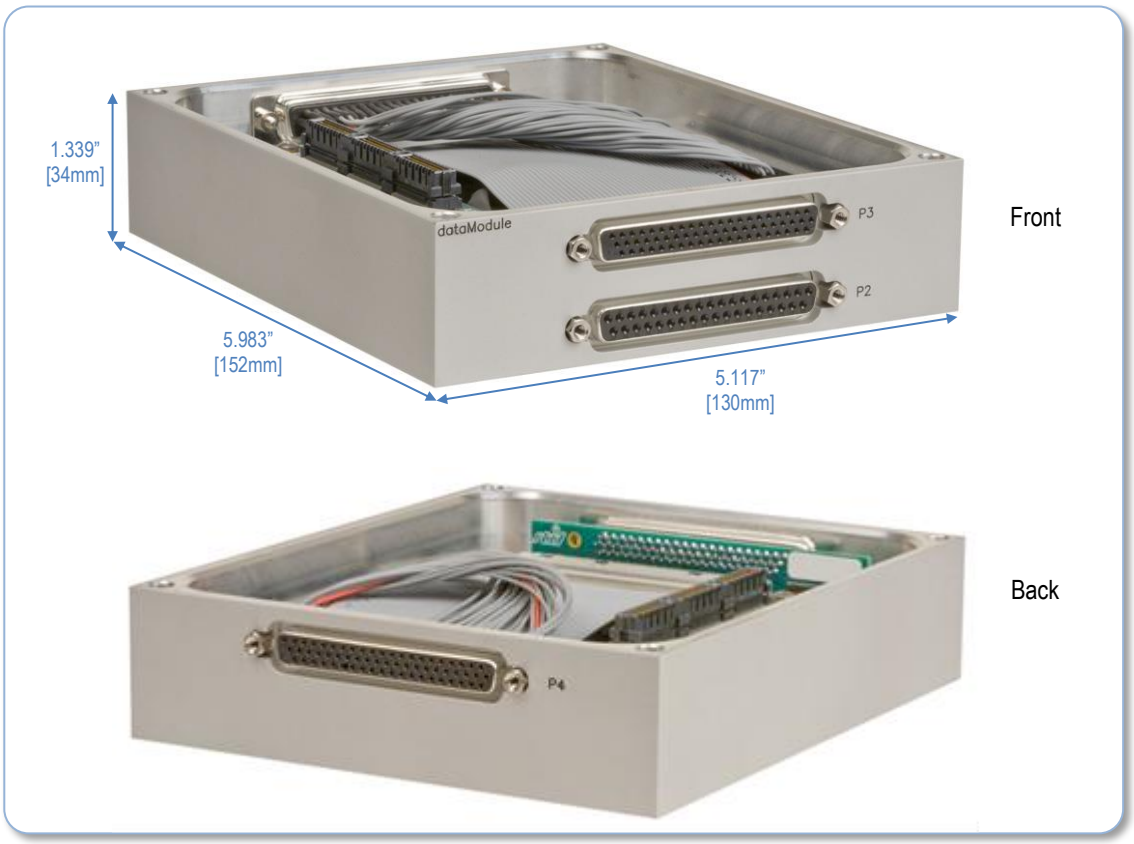

Figure 4: IDAN Dimensions

4.3 Connectors and Jumpers

P2: RS-232/422/485 Transceiver Connector

Connector Part #: Adam Tech DE37SD **Mating Connector:** Adam Tech DE37PD

Connector P2 provides configurable RS-232/422/485 transceivers. The pin configuration and associated FPGA signals are shown in the Table below. The signal names reflect the signal names in the Xilinx UCF file with the device pin out. For other modes, and information on how to configure the port, see Section 5.7 on page 25.

These signals are attached to Bank 2 of the FPGA, and should be configured as LVCMOS33.

Table 12: P2 Pin Assignments

IDAN P2 Pin		RS-232 Signal	Board Pin
Row 1	Row 2		
1		com1_dcd	CN10.1
	20	com1_dsr	CN10.2
2		com1_rxd	CN10.3
	21	com1_rtd	CN10.4
3		com1_txd	CN10.5
	22	com1_cts	CN10.6
4		com1_dtr	CN10.7
	23	com1_ri	CN10.8
5		GND	CN10.9
	24	com2_dcd	CN11.1
6		com2_dsr	CN11.2
	25	com2_rxd	CN11.3
7		com2_rtd	CN11.4
	26	com2_txd	CN11.5
8		com2_cts	CN11.6
	27	com2_dtr	CN11.7
9		com2_ri	CN11.8
	28	GND	CN11.9
10		com3_dcd	CN12.1
	29	com3_dsr	CN12.2
11		com3_rxd	CN12.3
	30	com3_rtd	CN12.4
12		com3_txd	CN12.5
	31	com3_cts	CN12.6
13		com3_dtr	CN12.7
	32	com3_ri	CN12.8
14		GND	CN12.9
	33	com4_dcd	CN13.1
15		com4_dsr	CN13.2
	34	com4_rxd	CN13.3
16		com4_rtd	CN13.4
	35	com4_txd	CN13.5
17		com4_cts	CN13.6
	36	com4_dtr	CN13.7
18		Com4_ri	CN13.8
	37	GND	CN13.9
19		n.c.	n.c.

P3: Digital I/O Connector

Connector Part #: VALCONN HDB-62S **Mating Connector:** VALCONN HDB-62P

Connector P3 provides 24 digital I/O lines, along with a +5V pin and ground pins. All I/O have pull up/pull down resistors that are controlled by jumper options, also shown in the table. These signals are 5V tolerant. The signal names reflect the signal names I n the Xilinx UCF file with the device pin out.

P3 is attached to Bank 0, and support any of the Spartan 6 I/O Standards that use a 3.3V V_{CCO} and no reference voltage. This includes LVTTL, LVCMOS33, and LVDS_33 input and output.

Connector P3 also provides a connection to the Xilinx JTAG programming header. This connector header mates with the Xilinx OEM programming cable through an adapter cable. The adapter cable is provided when purchasing the Starter Kit.

Table 13: P3 Pin Assignments

IDAN P3 Pin				Pull	
Row 1	Row 2	Row 3	Signal	Jmpr	C9 Pin
1			port1_p[0]	JP4	1
	22		GND		2
		43	port1_n[0]		3
2			GND		4
	23		port1_p[1]		5
		44	GND		6
3			port1_n[1]		7
	24		GND		8
		45	port1_p[2]		9
4			GND		10
	25		port1_n[2]		11
		46	GND		12
5			port1_p[3]		13
	26		GND		14
		47	port1_n[3]		15
6			GND		16
	27		port1_p[4]	JP5	17
		48	GND		18
7			port1_n[4]		19
	28		GND		20
		49	port1_p[5]		21
8			GND		22
	29		port1_n[5]		23
		50	GND		24
9			port1_p[6]		25
	30		GND		26
		51	port1_n[6]		27
10			GND		28
	31		port1_p[7]		29
		52	GND		30
11			port1_n[7]		31
	32		GND		32
		53	port1_p[8]	JP6	33
12			GND		34
	33		port1_n[8]		35
		54	GND		36
13			port1_p[9]		37
	34		GND		38
		55	port1_n[9]		39
14			GND		40
	35		port1_p[10]		41
		56	GND		42
15			port1_n[10]		43
	36		GND		44
		57	port1_p[11]		45
16			GND		46
	37		port1_n[11]		47
		58	GND		48
17			+5V		49
	38		GND		50
		59	*Reserved*		
18			jtag_vref		CN3.2
	39		GND		CN3.3

Table 13: P3 Pin Assignments

IDAN P3 Pin			Signal	Pull Jmpr	C9 Pin
Row 1	Row 2	Row 3			
		60	jtag_tms		CN3.4
19			GND_TCK		CN3.5
	40		jtag_tck		CN3.6
		61	GND		CN3.7
20			jtag_tdo		CN3.8
	41		GND		CN3.9
		62	jtag_tdi		CN3.10
21			*Reserved*		
	42		*Reserved*		

P4: High Speed Digital I/O Connector

Connector Part #: VALCONN HDB-62S **Mating Connector:** VALCONN HDB-62P

Connector P4 provides 40 digital I/O lines, along with a +5V pin and ground pins. These signals are 3.3V tolerant. The signal names reflect the signal names I n the Xilinx UCF file with the device pin out.

P4 is attached to Bank 1, and supports any of the Spartan 6 I/O Standards that use a 3.3V V_{CCO} and no reference voltage. This includes LVTTL, LVCMOS33 input and output, and LVDS_33 input. LVDS output is not supported in Bank 1.

Table 14: P4 Pin Assignments

IDAN P4 Pin			Signal	C8 Pin
Row 1	Row 2	Row 3		
1			Port2_p[0]	1
	22		Port2_n[0]	2
		43	Port2_p[1]	3
2			Port2_n[1]	4
	23		Port2_p[2]	5
		44	Port2_n[2]	6
3			Port2_p[3]	7
	24		Port2_n[3]	8
		45	GND	9
4			GND	10
	25		Port2_p[4]	11
		46	Port2_n[4]	12
5			Port2_p[5]	13
	26		Port2_n[5]	14
		47	Port2_p[6]	15
6			Port2_n[6]	16
	27		Port2_p[7]	17
		48	Port2_n[7]	18
7			GND	19
	28		GND	20
		49	Port2_p[8]	21
8			Port2_n[8]	22
	29		Port2_p[9]	23
		50	Port2_n[9]	24
9			Port2_p[10]	25
	30		Port2_n[10]	26
		51	Port2_p[11]	27
10			Port2_n[11]	28
	31		GND	29
		52	GND	30
11			Port2_p[12]	31
	32		Port2_n[12]	32
		53	Port2_p[13]	33
12			Port2_n[13]	34

Table 14: P4 Pin Assignments

IDAN P4 Pin				
Row 1	Row 2	Row 3	Signal	C8 Pin
	33		Port2_p[14]	35
		54	Port2_n[14]	36
13			Port2_p[15]	37
	34		Port2_n[15]	38
		55	GND	39
14			GND	40
	35		Port2_p[16]	41
		56	Port2_n[16]	42
15			Port2_p[17]	43
	36		Port2_n[17]	44
		57	Port2_p[18]	45
16			Port2_n[18]	46
	37		Port2_p[19]	47
		58	Port2_n[19]	48
17			+5V	49
	38		GND	50
		59	*Reserved*	
18			*Reserved*	
	39		*Reserved*	
		60	*Reserved*	
19			*Reserved*	
	40		*Reserved*	
		61	*Reserved*	
20			*Reserved*	
	41		*Reserved*	
		62	*Reserved*	
21			*Reserved*	
	42		*Reserved*	

4.3.1 BUS CONNECTORS

CN1(Top) & CN2(Bottom): PCIe Connector

The PCIe connector is the connection to the system CPU. The position and pin assignments are compliant with the *PCI/104-Express Specification*. (See PC/104 Specifications on page 35)

The FPGA35S6 is a "Universal" board, and can connect to either a Type 1 or Type 2 PCIe/104 connector.

4.3.2 JUMPERS

JP4, JP5, JP6: Pull up/Pull down Jumper

JP4, JP5, and JP6 are 3-pin two position jumpers that are used to set pull up or pull downs options on the I/O signal lines of CN9. Refer to Table 13 to determine which I/O pins are effected by each jumper.

Table 15: Pull up/Pull down Jumper options

Setting	Description
1-2	I/O is pulled up to 3.3V or 5V (Set by B1 and B2)
2-3	I/O is pulled down to GND
No Jumper	I/O has no pull up/pull down

JP1: Embedded Programmer Enable

This jumper is used to enable the embedded programmer to the JTAG chain. See Section 5.8 on page 26 for more details. The board can be programmed from and external programmer with this jumper in either position.

Table 16: JP1 – Embedded Programmer Enable

Setting	Description
1-2	Enabled embedded programmer
2-3 or open	Disables embedded programmer

JP8: User ID Jumper

The User ID Jumper is a four position, user defined jumper block. The jumpers can be read by the FPGA. An installed jumper results in a logic low, and an open jumper results in a logic high.

Table 17: JP8 – User ID Jumper

Position	Description
1-2	User ID bit 0
3-4	User ID bit 1
5-6	User ID bit 2
7-8	User ID bit 3

4.3.3 SOLDER JUMPER

B2: Pull up Voltage

Solder jumper B2 is used to set the pull up voltage for JP4, JP5 and JP6.

Table 18: B2 Pull up Voltage

Setting	Description
1-2	Sets Pull up voltage to 3.3V
2-3	Sets Pull up voltage to 5V

4.4 Steps for Installing

1. Always work at an ESD protected workstation, and wear a grounded wrist-strap.
2. Turn off power to the IDAN system.
3. Remove the module from its anti-static bag.
4. Check that pins of the bus connector are properly positioned.
5. Check the stacking order; make sure all of the busses used by the peripheral cards are connected to the cpuModule.
6. Hold the module by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
7. Gently and evenly press the module onto the IDAN system.
8. If any boards are to be stacked above this module, install them.
9. Finish assembling the IDAN stack by installing screws of an appropriate length.
10. Attach any necessary cables to the IDAN system.
11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working properly.

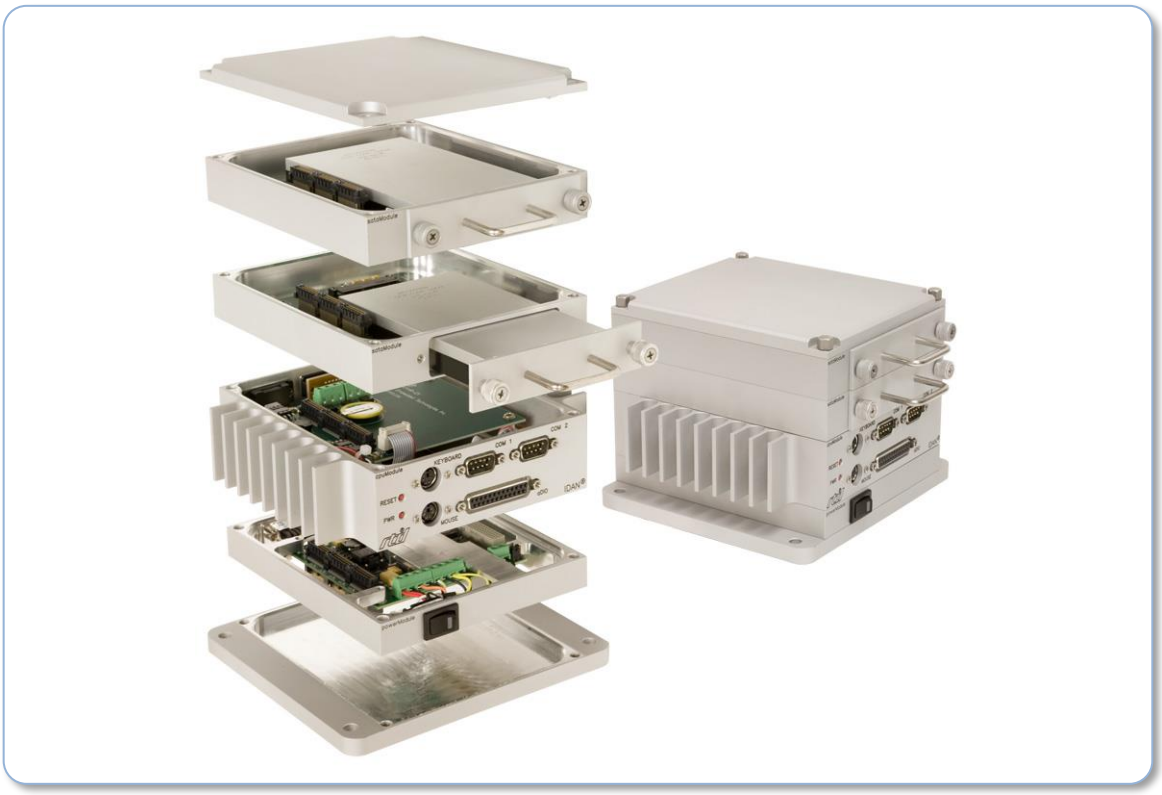

Figure 5: Example IDAN System

5 Functional Description

5.1 Block Diagram

The Figure below shows the functional block diagram of the FPGA35S6. The various parts of the block diagram are discussed in the following sections.

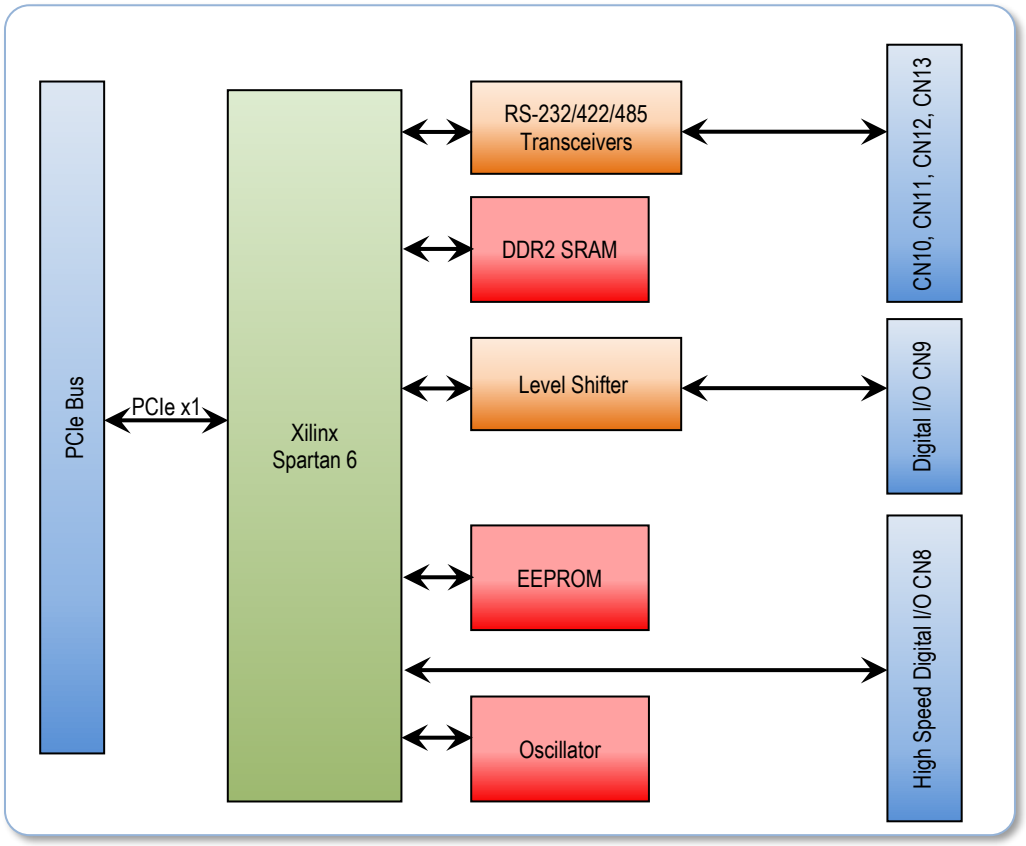

Figure 6: FPGA35S6 Block Diagram

5.2 Configuration Flash

The FPGA35S6 includes a Configuration Flash that is sized for the FPGA. At power up, the FPGA design is loaded from the Configuration Flash. The Configuration Flash can be programmed through either the Embedded Digilent® USB JTAG Programmer, or CN3: Xilinx JTAG Programming Header.

5.3 Oscillator

The FPGA35S6 features a 27Mhz oscillator for clock based operations in the FPGA.

5.4 EEPROM

The FPGA35S6 features a 256 x 16 SPI EEPROM, ATMEL AT93C66A. For information on the AT93C66A refer to http://www.atmel.com/

5.5 DDR2 SRAM

The FPGA35S6 features a 1Gb DDR2 SRAM, MT47H64M16HR 25E. This is interface to the Spartan 6 FPGA using Xilinx Memory Interface Generators (MIG) core. The example FPGA code has demonstrated how to use this core in a FPGA design.

5.6 Digital I/O

The FPGA35S6 digital I/O on connector CN9 uses the circuitry shown below to level shift the input voltage from 5V to 3.3V allowing the I/O to be 5V tolerant.

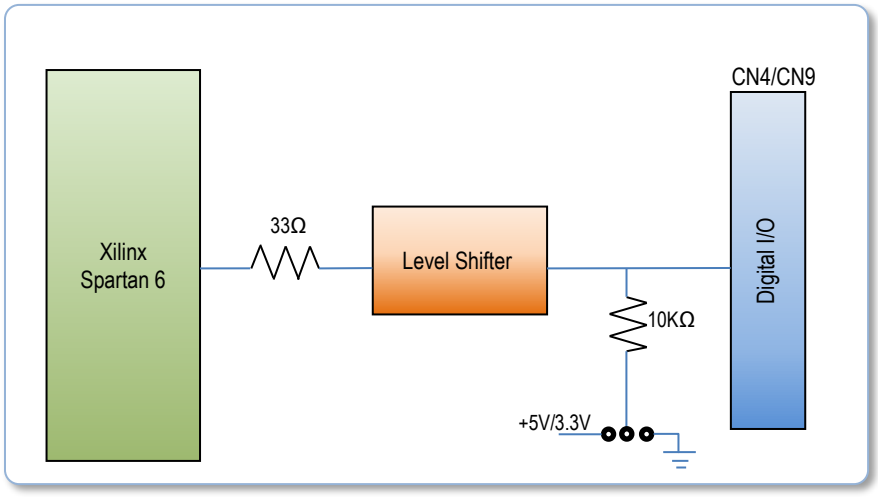

Figure 7: CN9 Digital I/O Circuitry

5.7 RS-232/422/485 Transceivers

The RS-232/422/485 transceivers on this board all it to interface with a variety of serial port standards, incremental encoders, and other devices. The transceivers are highly configurable from the FPGA fabric. The Figure below shows the connections between the FPGA signals, the Exar SP338 transceiver, and the connector.

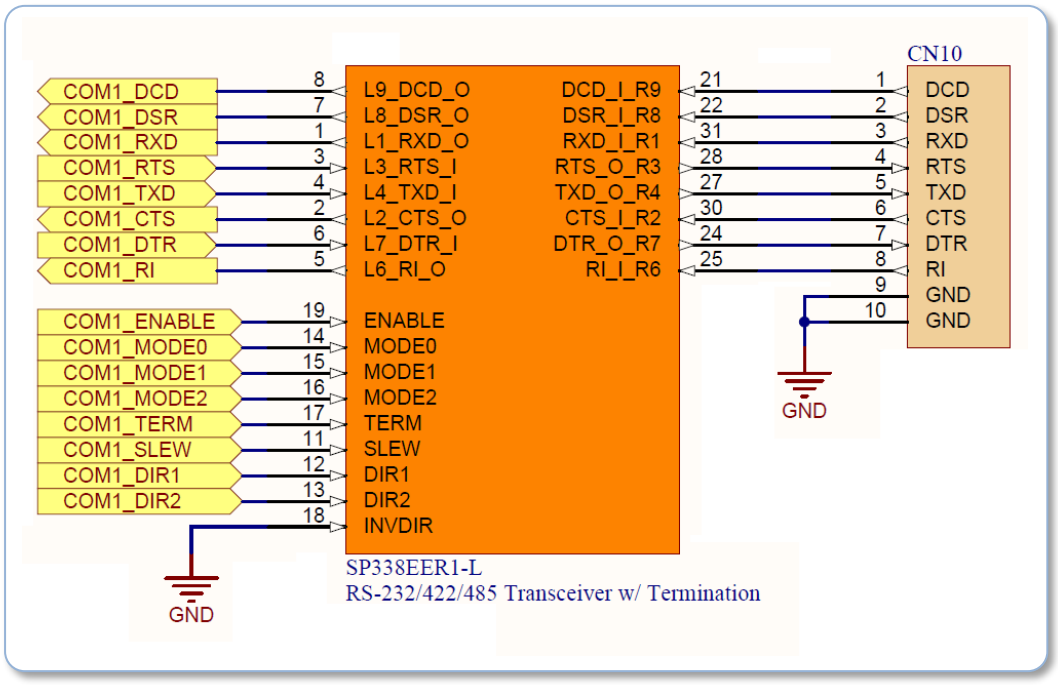

Figure 8: Serial Port Transceiver

The various modes are show in Table 19 below. The modes are selected using the com?_mode[2:0] signals in the FPGA. The Table then shows the FPGA signal associated with each pin of the connector.

Table 19: Transceiver Configuration

	RS-232 **com?_mode[2:0]** = 001		**RS-485** **com?_mode[2:0]** = 010		**RS-422** **com?_mode[2:0]** = 011		**Dual RS-422** **com?_mode[2:0]** = 100		**Dual RS-485** **com?_mode[2:0]** = 111	
CN Pin	**FPGA Signal**	**Use**	**FPGA Signal**	**Use**	**FPGA Signal**	**Use**	**FPGA Signal**	**Use**	**FPGA Signal**	**Use**
1	**com?_dcd** (RX)	DCD	*	D-	*	TXD-	*	TXD1-	*	D1-
2	**com?_dsr** (RX)	DSR					*	TXD2-	*	D2-
3	**com?_rxd** (RX)	RXD	**com?_dcd** (RX) **com?_txd** (TX)	D+	**com?_txd** (TX)	TXD+	**com?_txd** (TX)	TXD1+	**com?_dcd** (RX) **com?_txd** (TX)	D1+
4	**com?_rtd** (TX)	RTS					**com?_dtr** (TX)	TXD2+	**com?_cts** (RX) **com?_dtr** (TX)	D2+
5	**com?_txd** (TX)	TXD			**com?_dcd** (RX)	RXD+	**com?_dcd** (RX)	RXD1+	**com?_dsr** (RX)	RXD4+
6	**com?_cts** (RX)	CTS					**com?_rxd** (RX)	RXD2+	**com?_ri** (RX)	RXD3+
7	**com?_dtr** (TX)	DTR			*	RXD-	*	RXD1-	*	RXD4-
8	**com?_ri** (RX)	RI					*	RXD2-	*	RXD3-
	com?_dir1		'1' = D Transmitting '0' = D Receiving		'1' = TXD enabled '0' = TXD disabled		'1' = TXD1 enabled '0' = TXD1 disabled		'1' = D1 Transmitting '0' = D1 Receiving	
	com?_dir2						'1' = TXD2 enabled '0' = TXD2 disabled		'1' = D2 Transmitting '0' = D2 Receiving	

The other signals that are used to configure the transceivers are below:

com?_enable: '1' for normal operation, '0' for shutdown mode
com?_slew: '1' for 250 kbps slew limiting, '0' for full speed operation
com?_term: '1' to enable receiver termination (RS-422/485 modes only), '0' to disable termination

5.8 Embedded Digilent® USB JTAG Programmer

This FPGA board includes an embedded Digilent ® JTAG programming module. It connects to the host through the USB connections on the PCIe Bus connectors. A USB hub is also provided for lane repopulation. The programming module is compatible with all Xilinx tools, including iMpact and ChipScope (www.xilinx.com). It is also supported by Digilent's Adept software package (www.digilentinc.com).

In order to use the embedded programmer, JP1 must be installed. This attaches the programmer to the JTAG chain. CN3 can always be used regardless of whether or not JP1 is installed.

The embedded programmer has a user string of "RTD" followed by the serial number of the board. This can be used to differentiate the programmers if there are multiple boards in the system.

6 Register Address Space

This is the register address space for the example FPGA that is given with the FPGA35S6.

6.1 Identifying the Board

The FPGA35S6 Example shows up in standard PCI Configuration space as a PCI device. It can be positively identified as shown in the Table below.

Table 20: Identifying the FPGA35S6

Configuration Space Offset	Register Description	Value
0x00	Vendor ID	0x1435
0x02	Device ID	0x5800

6.2 BAR0 – FPGA Example Register Map

Table 21: FPGA Example Register Map

Offset	0x03	0x02	0x01	0x00
0x00	R_ID			
0x04	R_STATUS			
0x08	R_EEPROM			
0x0C	R_USER_ID			
0x20	R_PORT1_IN			
0x24	R_PORT1_OUT			
0x28	R_PORT1_DIR			
0x30	R_PORT2L_IN			
0x34	R_PORT2L_OUT			
0x38	R_PORT2L_DIR			
0x40	R_PORT2H_IN			
0x44	R_PORT2H_OUT			
0x48	R_PORT2H_DIR			
0x50	R_DDR_RD_DATA			
0x54	R_DDR_WR_DATA			
0x58	R_DDR_ADDR			
0x5C	R_DDR_STATUS			
0x60	R_CLK_27_1			
0x64	R_CLK_27_2			
0x70	R_COM1_OUT			
0x74	R_COM1_IN			
0x78	R_COM2_OUT			
0x7C	R_COM2_IN			
0x80	R_COM3_OUT			
0x84	R_COM3_IN			
0x88	R_COM4_OUT			
0x8C	R_COM4_IN			

6.2.1 R_ID (READ)

This is a register that identifies the board.

0x12345678 is the identification of the example code

6.2.2 R_STATUS (READ)

This is a status register for power good (pgood) for the power supplies and serial out from the EEPROM

B0: EEPROM Serial out

B4: 1.2V pgood

B5: 1.8V pgood

B6: 3.3V pgood

6.2.3 R_EEPROM (READ/WRITE)

This register has the outputs to the EEPROM.

B0: EEPROM Serial Clock

B1: EEPROM Serial Input

B2: EEPROM Chip Select

6.2.4 R_USER_ID (READ)

This register shows the status of the User ID Jumpers

B0: User ID 0 Jumper. 0 = Open, 1 = Closed

B1: User ID 1 Jumper. 0 = Open, 1 = Closed

B2: User ID 2 Jumper. 0 = Open, 1 = Closed

B3: User ID 3 Jumper. 0 = Open, 1 = Closed

6.2.5 R_PORT1_IN (READ)

This is the input register for the port1. This reads the current value the I/O.

6.2.6 R_PORT1_OUT (WRITE)

This is the output register for the port1. The value to be output, direction must be set to output.

6.2.7 R_PORT1_DIR (READ/WRITE)

This is the direction register for port1. Indicates the direction of each pin '0' = input '1' = output

6.2.8 R_PORT2L_IN (READ)

This is the input register for the port2 low, port2_[0]…port2_[15] . This reads the current value the I/O.

6.2.9 R_PORT2L_OUT (WRITE)

This is the output register for the port2 low, port2_[0]…port2_[15]. The value to be output, direction must be set to output.

6.2.10 R_PORT2L_DIR (READ/WRITE)

This is the direction register for port2 low, port2_[0]…port2_[15]. Indicates the direction of each pin '0' = input '1' = output

6.2.11 R_PORT2H_IN (READ)

This is the input register for the port2 high, port2_[16]…port2_[19]. This reads the current value the I/O.

6.2.12 R_PORT2H_OUT (WRITE)

This is the output register for the port2 high, port2_[16]…port2_[19]. The value to be output, direction must be set to output.

6.2.13 R_PORT2H_DIR (READ/WRITE)

This is the direction register for port2 high, port2_[16]…port2_[19]. Indicates the direction of each pin '0' = input '1' = output

6.2.14 R_DDR_RD_DATA (READ)

Reads the data of the DDR2 SRAM at R_DDR_ADDR location

A read is performed by writing address to R_DDR_ADDR.

6.2.15 R_DDR_WR_DATA (READ/WRITE)

Writes data in registry to location R_DDR_ADDR of the DDR2 SRAM

6.2.16 R_DDR_ADDR (READ/WRITE)

Address pointer of the DDR2 SRAM.

6.2.17 R_DDR_STATUS (READ)

This is a status register for the DDR2 memory interface.

B0: Read error

B1: Read overflow

B2: Read empty

B3: Read full

B4: Write error

B5: Write underrun

B6: Write empty

B7: Write full

B[14:8]: Read count

B[22:16]: Write count

B[24]: Command full

B[25]: Command empty

B[31]: Calibration done

6.2.18 R_COM1_OUT (READ/WRITE)

This register sets the configuration and outputs of CN10 RS-232/422/485 transceivers.

B0: com1_txd

B1: com1_rts

B2: com1_dtr

B8: com1_enable

B9: com1_mode0

B10: com1_mode1

B11: com1_mode2

B12: com1_dir1

B13: com1_dir2

B14: com1_slew

B15: com1_term

6.2.19 R_COM1_IN (READ)

This register reads the inputs of CN10 RS-232/422/485 transceivers.

B0: com1_rxd

B1: com1_cts

B2: com1_dsr

B3: com1_dcd

B7: com1_ri

6.2.20 R_COM2_OUT (READ/WRITE)

This register sets the configuration and outputs of CN11 RS-232/422/485 transceivers.

B0: com2_txd

B1: com2_rts

B2: com2_dtr

B8: com2_enable

B9: com2_mode0

B10: com2_mode1

B11: com2_mode2

B12: com2_dir1

B13: com2_dir2

B14: com2_slew

B15: com2_term

6.2.21 R_COM2_IN (READ)

This register reads the inputs of CN11 RS-232/422/485 transceivers.

B0: com2_rxd

B1: com2_cts

B2: com2_dsr

B3: com2_dcd

B7: com2_ri

6.2.22 R_COM3_OUT (READ/WRITE)

This register sets the configuration and outputs of CN12 RS-232/422/485 transceivers.

B0: com3_txd

B1: com3_rts

B2: com3_dtr

B8: com3_enable

B9: com3_mode0

B10: com3_mode1

B11: com3_mode2

B12: com3_dir1

B13: com3_dir2

B14: com3_slew

B15: com3_term

6.2.23 R_COM3_IN (READ)

This register reads the inputs of CN12 RS-232/422/485 transceivers.

B0: com3_rxd

B1: com3_cts

B2: com3_dsr

B3: com3_dcd

B7: com3_ri

6.2.24 R_COM4_OUT (READ/WRITE)

This register sets the configuration and outputs of CN13 RS-232/422/485 transceivers.

B0: com4_txd

B1: com4_rts

B2: com4_dtr

B8: com4_enable

B9: com4_mode0

B10: com4_mode1

B11: com4_mode2

B12: com4_dir1

B13: com4_dir2

B14: com4_slew

B15: com4_term

6.2.25 R_COM4_IN (READ)

This register reads the inputs of CN13 RS-232/422/485 transceivers.

B0: com4_rxd

B1: com4_cts

B2: com4_dsr

B3: com4_dcd

B7: com4_ri

7 Troubleshooting

If you are having problems with your system, please try the following initial steps:

- **Simplify the System** – Remove modules one at a time from your system to see if there is a specific module that is causing a problem. Perform you troubleshooting with the least number of modules in the system possible.

- **Swap Components** – Try replacing parts in the system one at a time with similar parts to determine if a part is faulty or if a type of part is configured incorrectly.

If problems persist, or you have questions about configuring this product, contact RTD Embedded Technologies via the following methods:

Phone: +1-814-234-8087
E-Mail: techsupport@rtd.com

Be sure to check the RTD web site (http://www.rtd.com) frequently for product updates, including newer versions of the board manual and application software.

8 Additional Information

8.1 PC/104 Specifications

A copy of the latest PC/104 specifications can be found on the webpage for the PC/104 Embedded Consortium:

www.pc104.org

8.2 PCI and PCI Express Specification

A copy of the latest PCI and PCI Express specifications can be found on the webpage for the PCI Special Interest Group:

www.pcisig.com

8.3 Serial Port Transceivers

Detailed information on the Exar SP338 serial port transceivers is available on the Exar website:

www.exar.com/connectivity/transceiver/multiprotocol/sp338

9 Limited Warranty

RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD Embedded Technologies, Inc. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, RTD Embedded Technologies will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to RTD Embedded Technologies. All replaced parts and products become the property of RTD Embedded Technologies. Before returning any product for repair, customers are required to contact the factory for a Return Material Authorization (RMA) number.

This limited warranty does not extend to any products which have been damaged as a result of accident, misuse, abuse (such as: use of incorrect input voltages, improper or insufficient ventilation, failure to follow the operating instructions that are provided by RTD Embedded Technologies, “acts of God” or other contingencies beyond the control of RTD Embedded Technologies), or as a result of service or modification by anyone other than RTD Embedded Technologies. Except as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranties of merchantability and fitness for a particular purpose, and RTD Embedded Technologies expressly disclaims all warranties not stated herein. All implied warranties, including implied warranties for merchantability and fitness for a particular purpose, are limited to the duration of this warranty. In the event the product is not free from defects as warranted above, the purchaser's sole remedy shall be repair or replacement as provided above. Under no circumstances will RTD Embedded Technologies be liable to the purchaser or any user for any damages, including any incidental or consequential damages, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

Some states do not allow the exclusion or limitation of incidental or consequential damages for consumer products, and some states do not allow limitations on how long an implied warranty lasts, so the above limitations or exclusions may not apply to you.

This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

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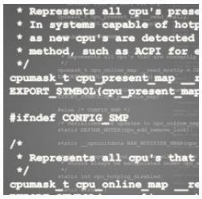

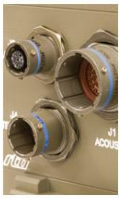
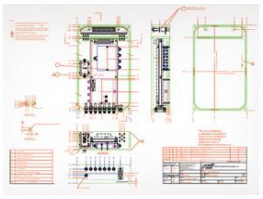

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